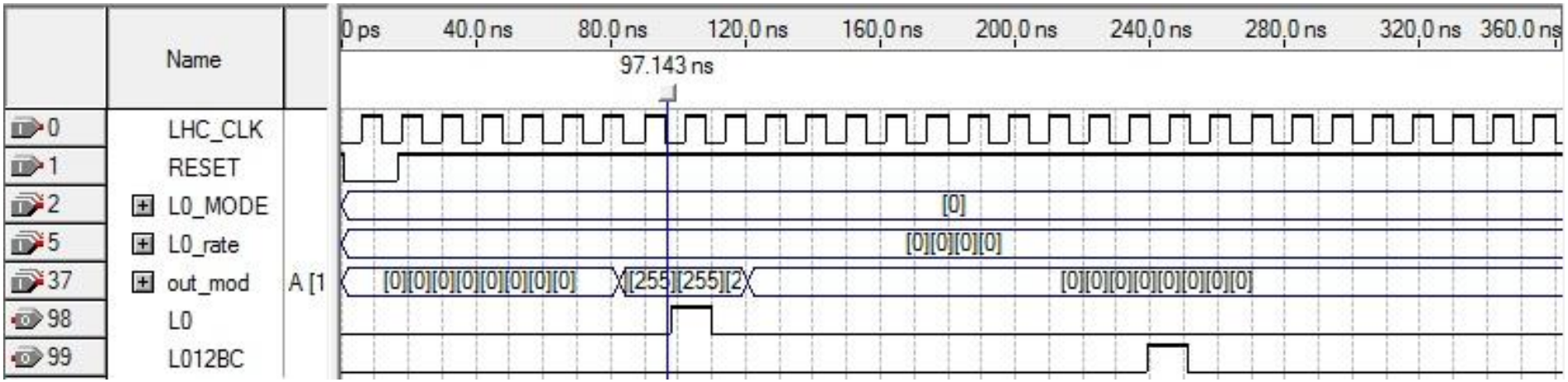
Reporte de Actividades

Guillermo Tejeda Muñoz

8-06-2012

Delay



Delay de 12 BC

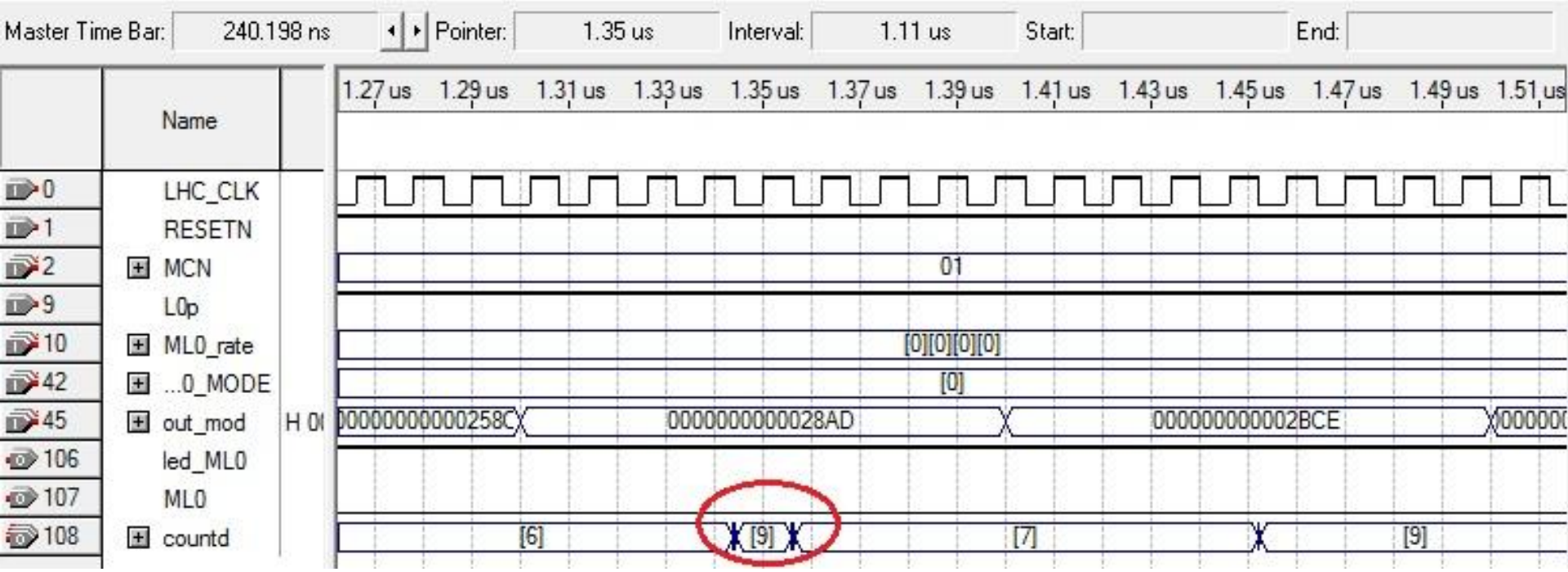
Funciones:

- L0
- Random
- Toogle
- Signature

Firmware

- Salidas para Tarjeta en Caverna:
  - L0
  - ML0
  - ML0
  - BUSY
  - ML0
  - ML0
- TERMINADO (Todas las funciones)

Pruebas de generación de ML0



Algunas partes de la suma tienen un estado incorrecto.

L0 y ML0

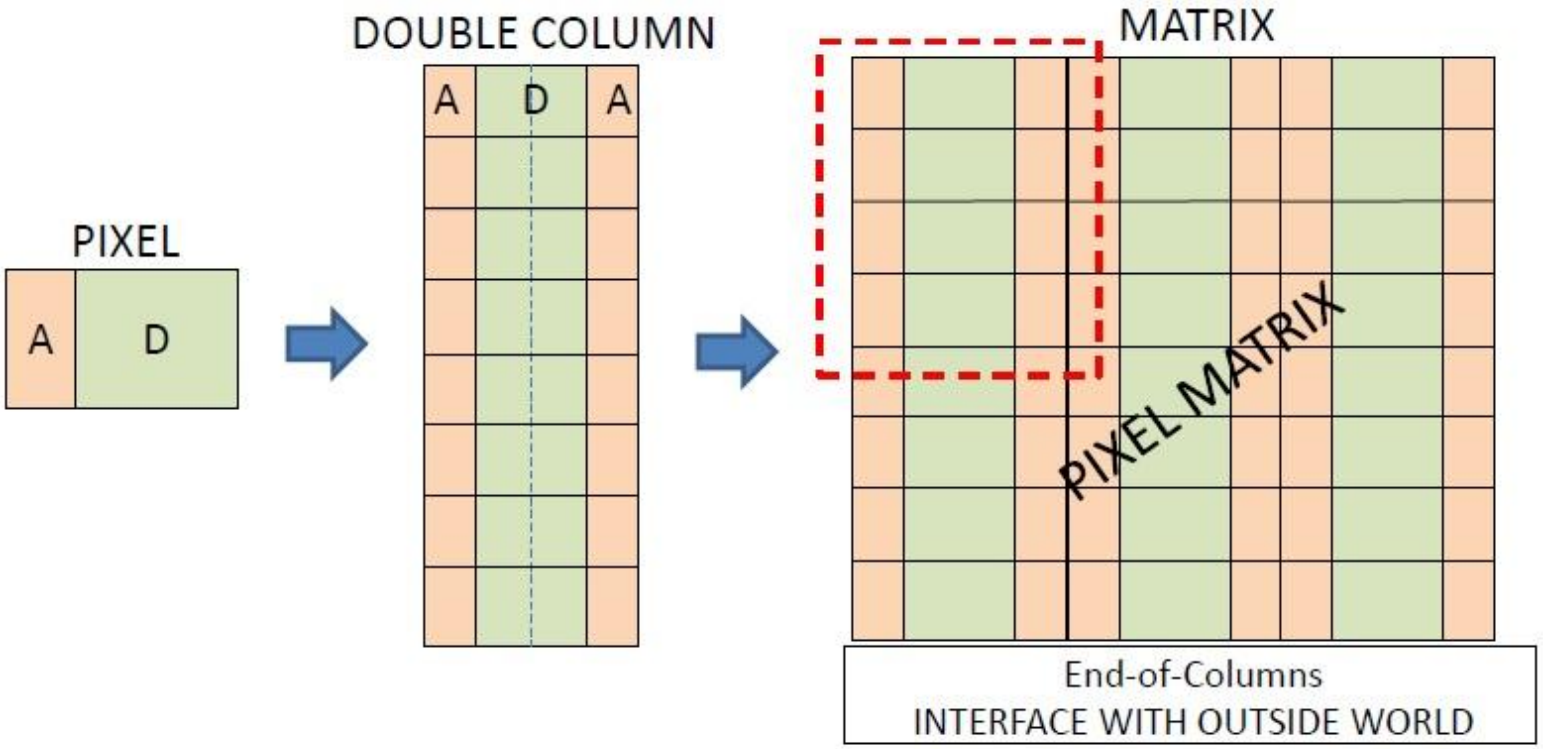
- Generados a partir de dos bloques de datos diferentes.
- Cada bloque tiene diferentes reestricciones de tiempos (Reset).
- Si:
  - ML0 = trigger, L0 sin función.

Resúmenes (22 Junio)

- Tesis de Luis (*)
- APD (*)
- Contadora (*)
- PC
- Cubo

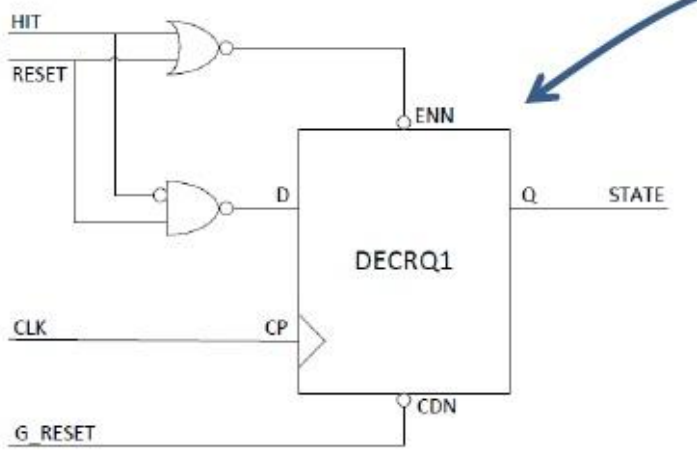
ITS Upgrade

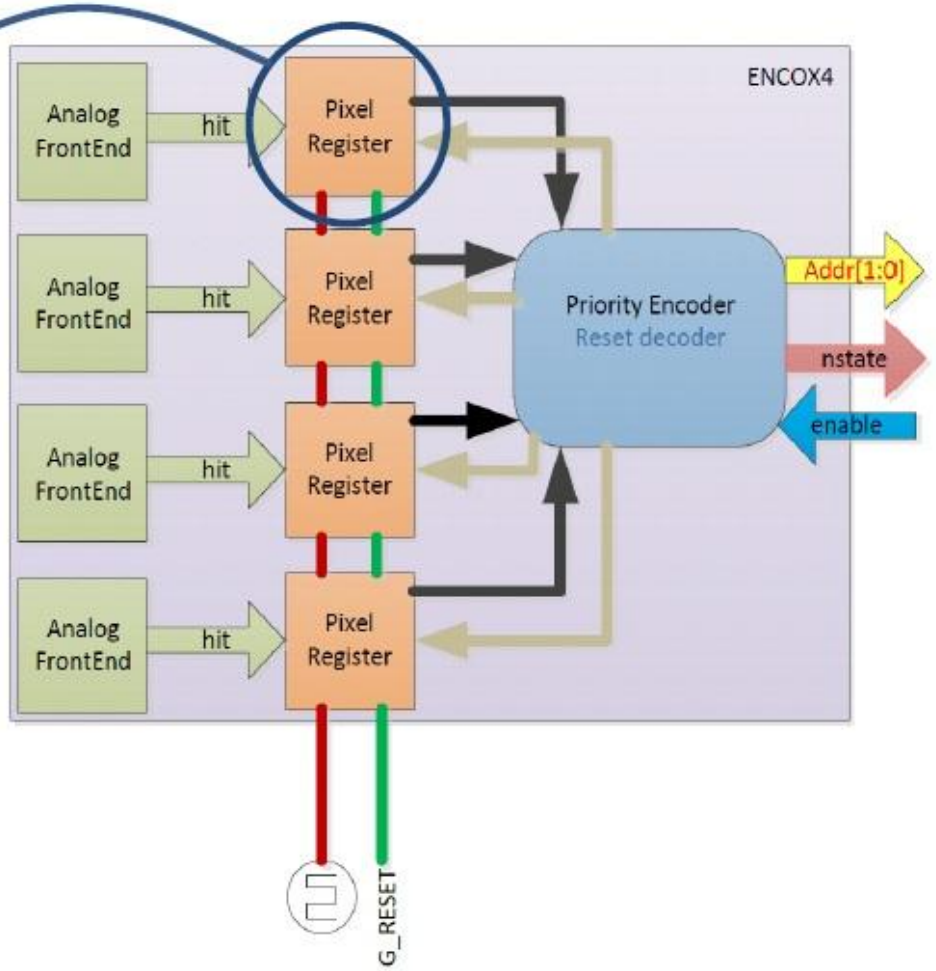
ReadOut



- Matrix of pixels arranged in columns: 2 adjacent, mirrored, columns share the same digital area
- GOAL: after a trigger, read only the active pixels, and reset them
- Possible readout architecture with priority encoder -> basic cell of 4 pixels, repeated to read larger structures

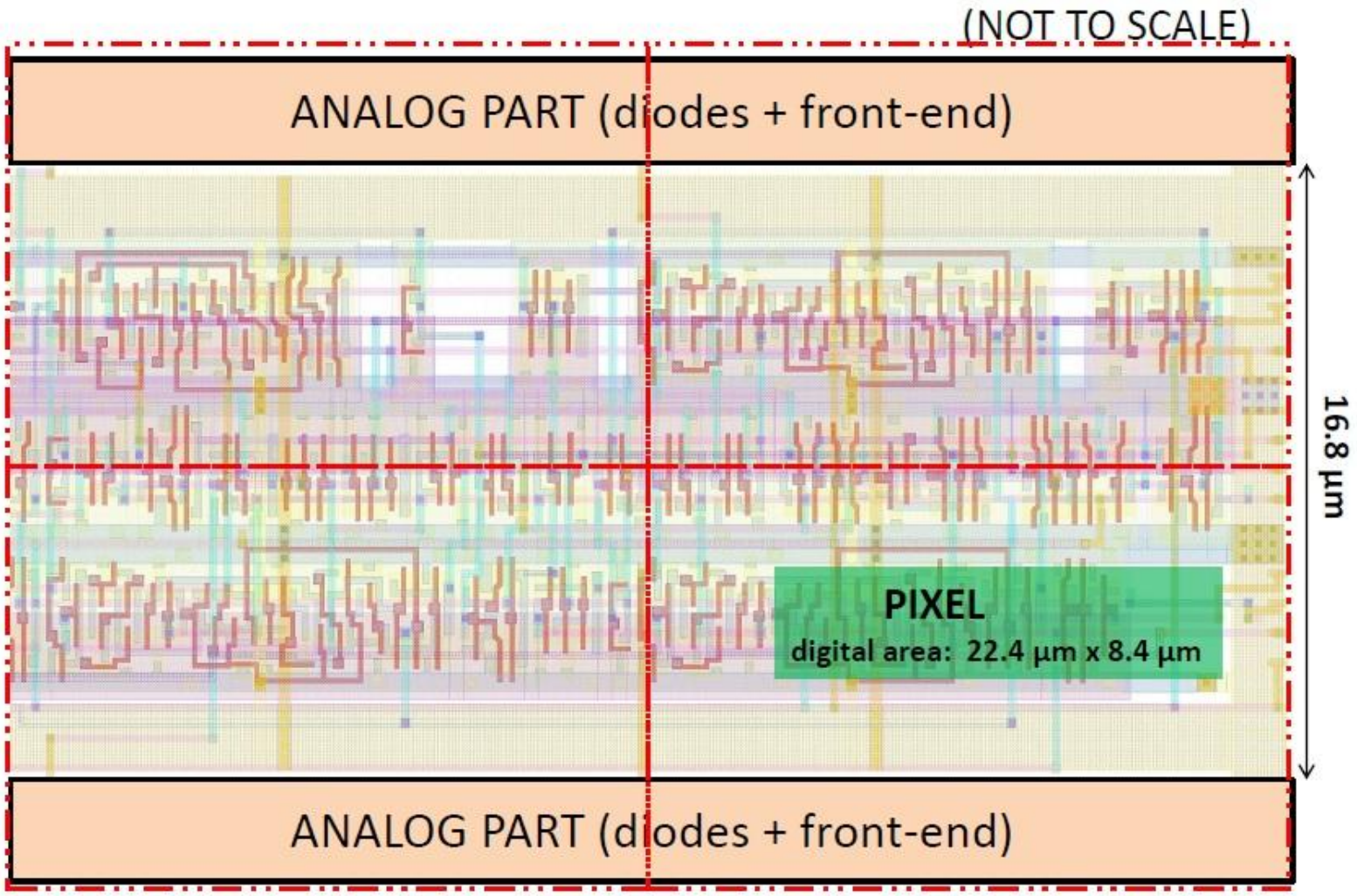
Synchronous readout





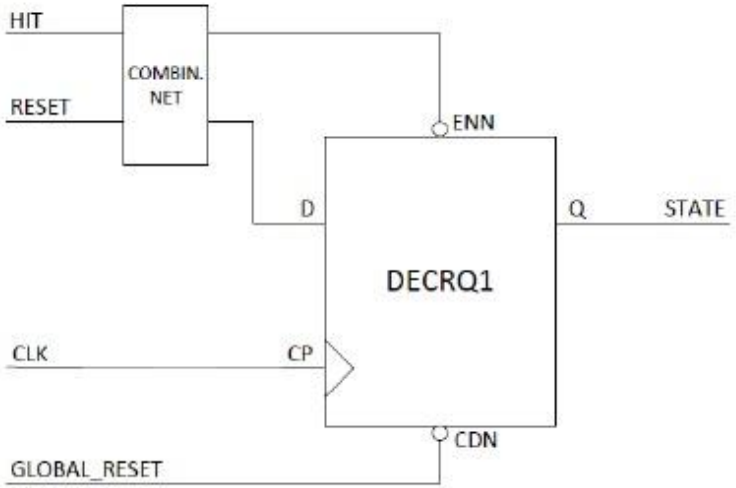
- Clock + global reset propagated through the full matrix
- Address + nstate (global OR) sent to EoC for elaboration/readout
- Read enable signal sent back from EoC
- After synthesis (x 16 pixels):
  - total area = 3060 µm²
  - per pixel ~191.25 µm²

Layout


(NOT TO SCALE)
ANALOG PART (diodes + front-end)
PIXEL
digital area: 22.4 µm x 8.4 µm
16.8 µm
ANALOG PART (diodes + front-end)

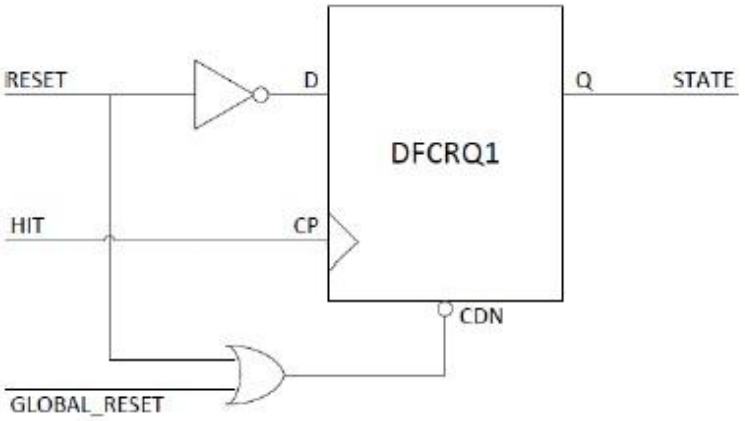
Hit

SYNCHRONOUS



- ✓ easy encoding of synch hit data
- ✓ few logic and small pixel area (only 1 FF)
- ✗ necessity to propagate the clock to the full matrix -> switching problems, power consumption

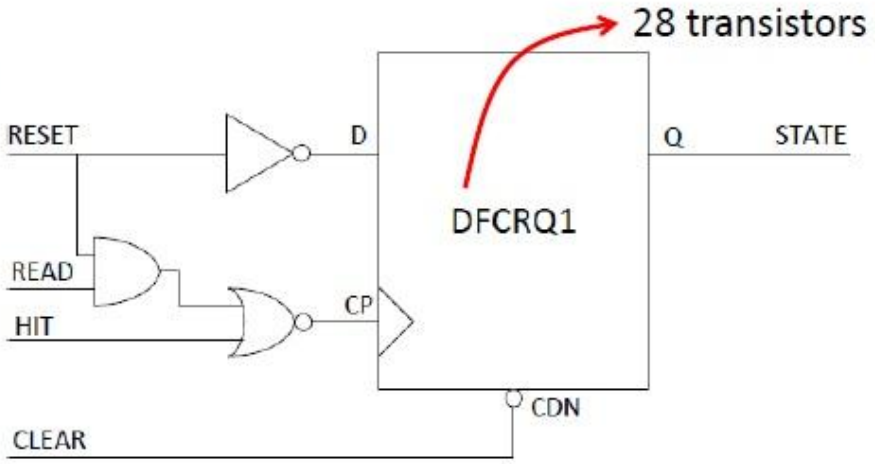
ASYNCHRONOUS "TOGGLE"



- ✓ no clock propagation -> lower power consumption
- ✓ asynch. hit encoding
- ✗ more logic to ensure proper reset, larger pixel area

Gated Hit

- The FF is sensible to the edge of RESET signal -> register reset at the end of the reset pulse
- Must ensure that CP variation happens AFTER D variation



- Studies on custom architectures for the flip-flop
  - FF with NAND gates
  - latch with pulse generators