

Reporte de Actividades

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1-6-2012

ACORDE 1/3

- Delay 12 BC
 - > 94 % recursos internos utilizados
 - **Salidas actuales**
 - 1 L0
 - 2 ML0
 - 3 (57 & 58)
 - 4 Busy
 - 5
 - 6
 - **Propuesta**
 - 1 L0
 - 2 ML0
 - 3 ML0 (nuevo)
 - 4 Busy
 - 5 L0 (+ 12 BC)
 - 6 ML0 (nuevo y dif. conv.)

ACORDE 2/3

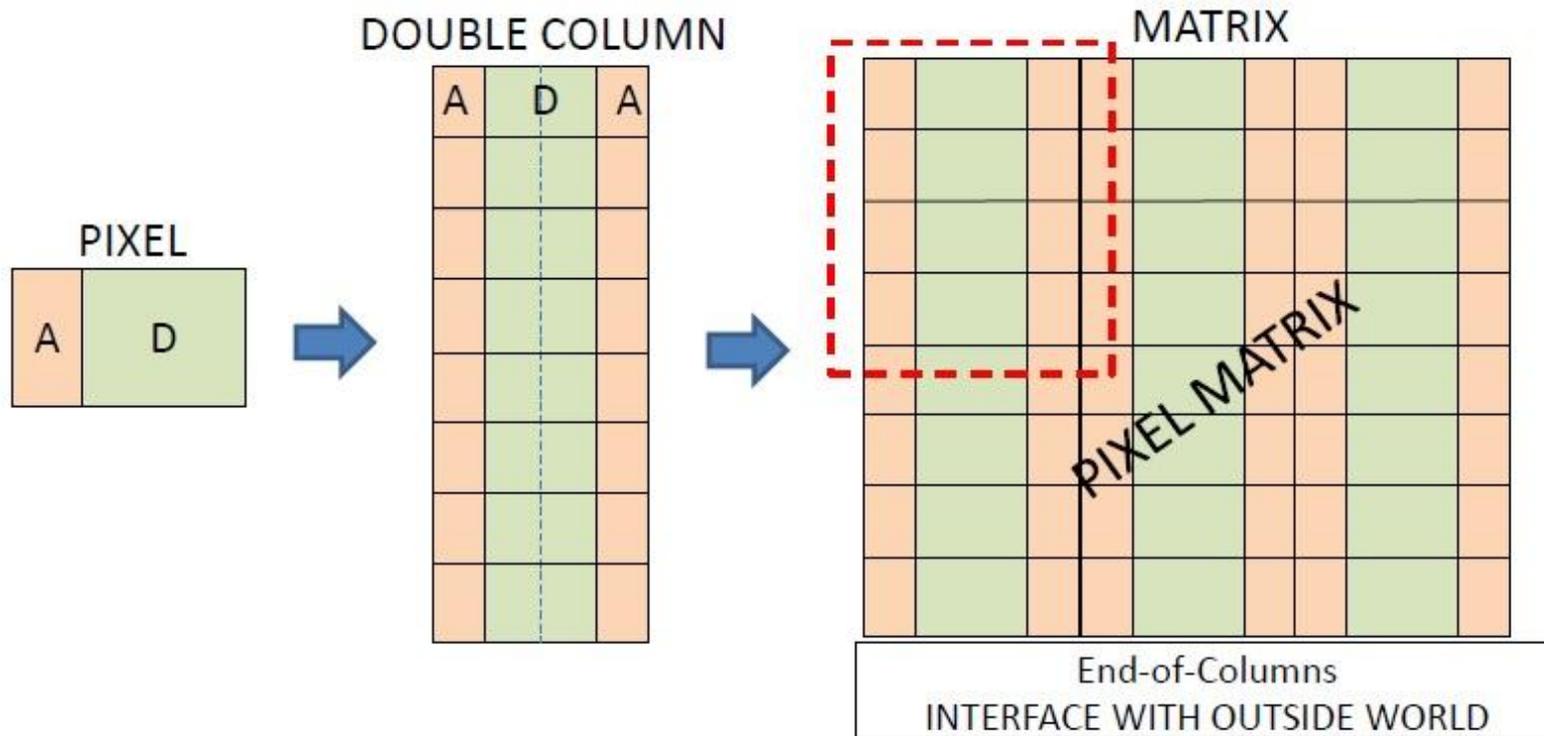
- Agregar un nuevo L0 con un delay de 12BC:
 - L0
 - Random
 - Signature
 - Toogle
- Solo L0 +12BC:
 - Incremento al 96% de recursos (máquina de estados)
- L0 + Random:
 - 101%

ACORDE 3/3

- Problemas con delays (Timing constraints)
 - Revisar manuales de TTC y SIU para definir los tiempos en el FPGA (nuevos).
 - Realizar los cambios para tener las salidas propuestas.
 - No se podrán hacer pruebas.

Info Extra

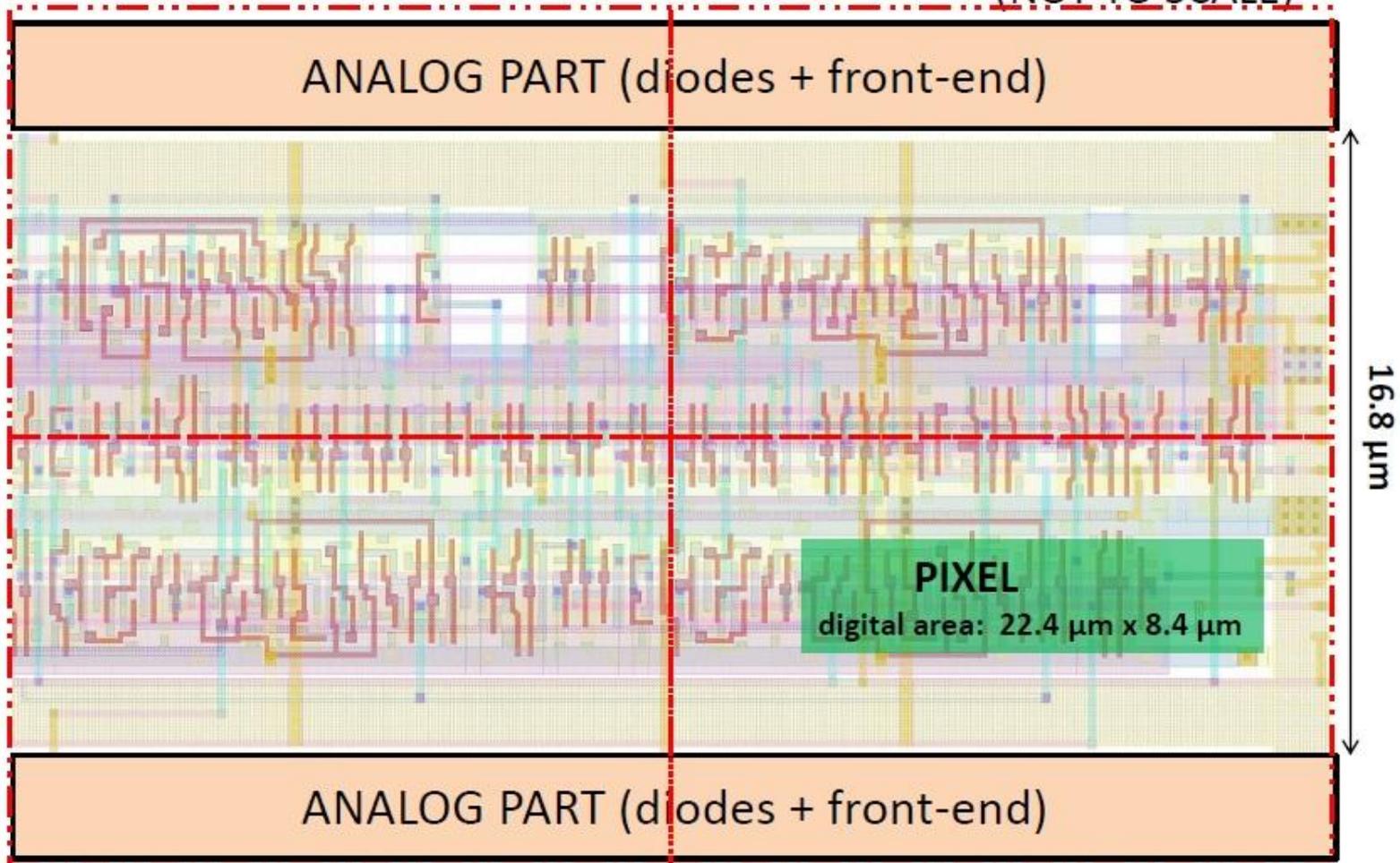
ReadOut



- Matrix of pixels arranged in columns: 2 adjacent, mirrored, columns share the same digital area
- **GOAL:** after a trigger, read only the active pixels, and reset them
- Possible readout architecture with priority encoder -> basic cell of 4 pixels, repeated to read larger structures

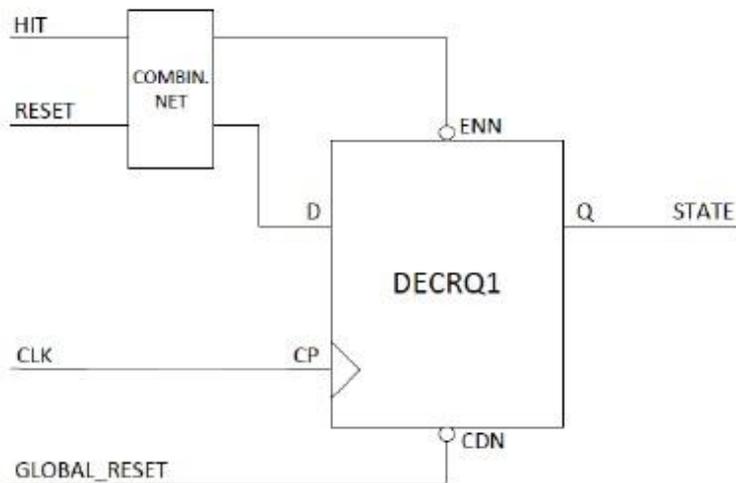
Layout

(NOT TO SCALE)



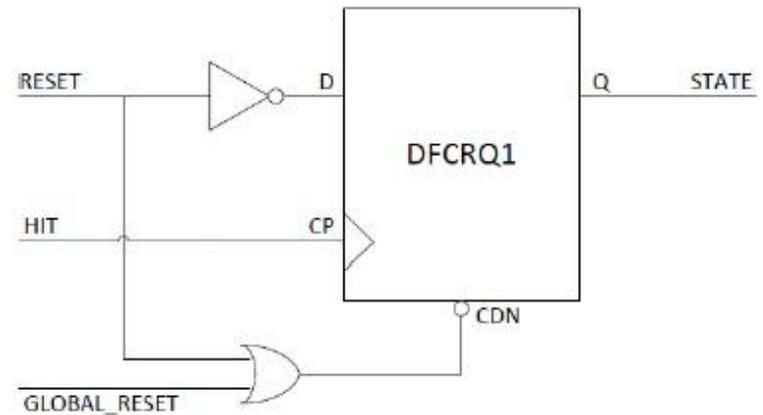
Hit

SYNCHRONOUS



- ✓ • easy encoding of synch hit data
- ✓ • few logic and small pixel area (only 1 FF)
- ✗ • necessity to propagate the clock to the full matrix -> switching problems, power consumption

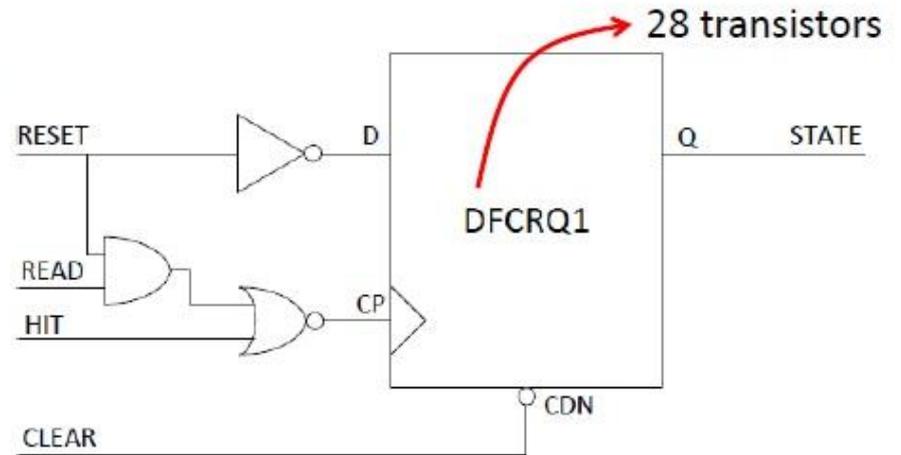
ASYNCHRONOUS "TOGGLE"



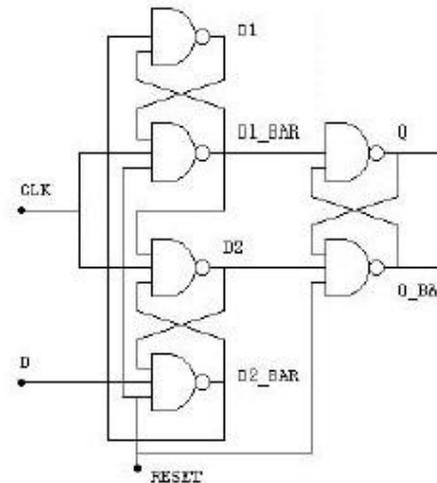
- ✓ • no clock propagation -> lower power consumption
- ✓ • asynch. hit encoding
- ✗ • more logic to ensure proper reset, larger pixel area

Gated Hit

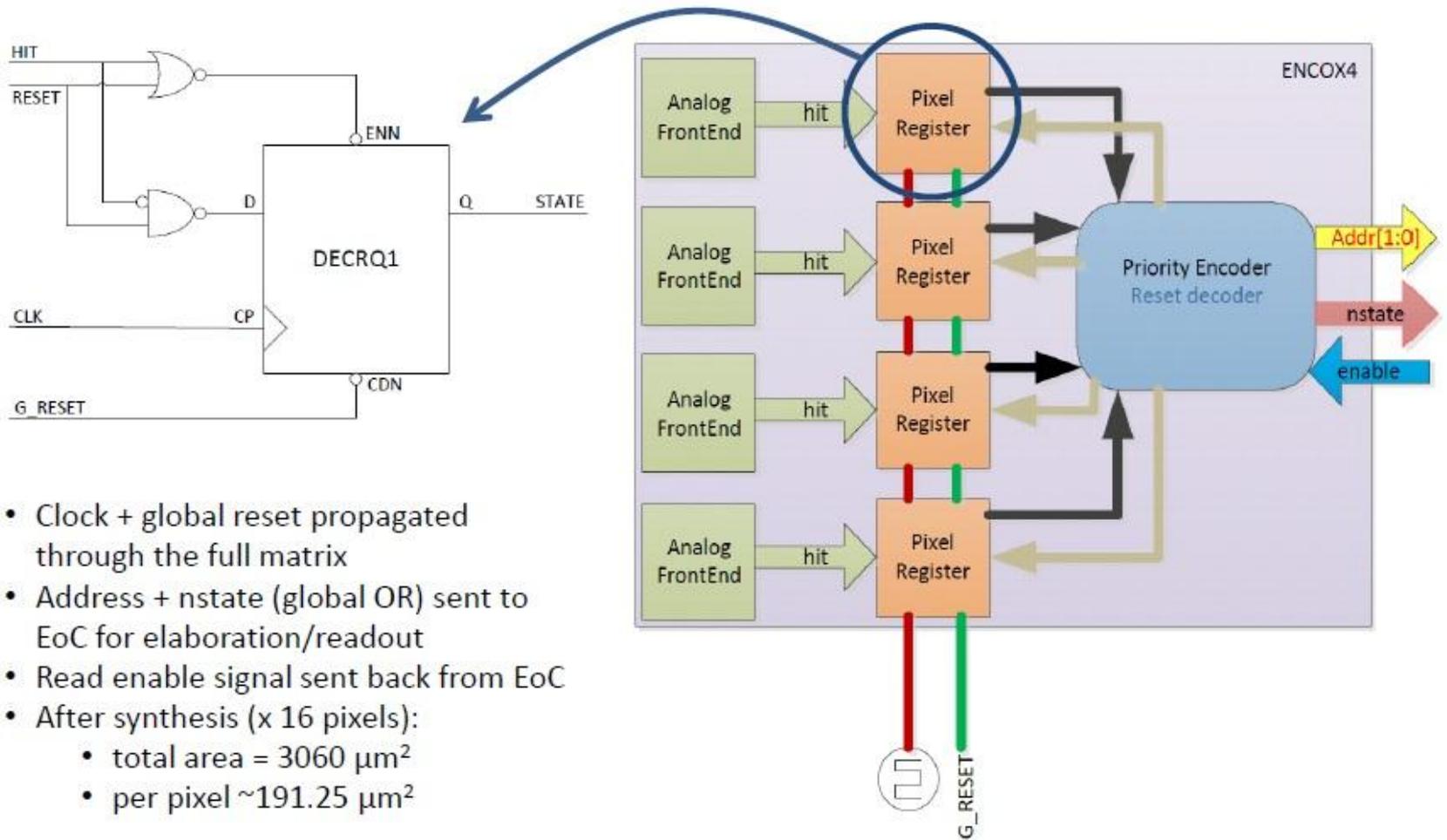
- The FF is sensible to the edge of RESET signal -> register reset at the end of the reset pulse
- Must ensure that CP variation happens AFTER D variation



- Studies on custom architectures for the flip-flop
 - FF with NAND gates
 - latch with pulse generators



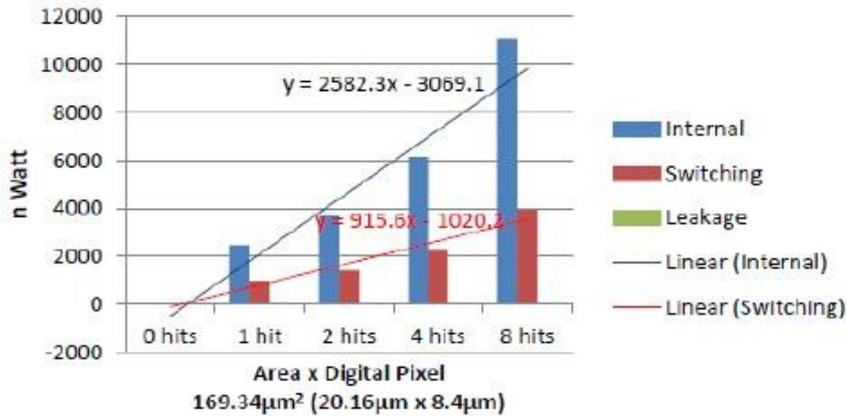
Synchronous readout



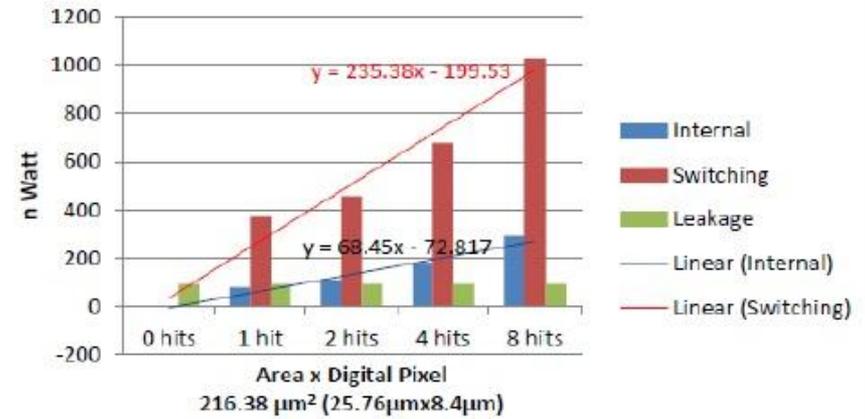
- Clock + global reset propagated through the full matrix
- Address + nstate (global OR) sent to EoC for elaboration/readout
- Read enable signal sent back from EoC
- After synthesis (x 16 pixels):
 - total area = 3060 μm^2
 - per pixel $\sim 191.25 \mu\text{m}^2$

Power consumption

Sync



FF@Address



Toggle

