The modern concept of recording system elements for the INCA project

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Abstract: The modern concept of elements of recording system elements for the INCA project instrument designed to study the primary cosmic radiation up to energies of $\sim 10^{16}$ eV is considered. A multichannel analog-to-digital conversion system with a wide dynamical band (10^6), a system of registration of "Helium-2" neutron-counter signals, a time scanning system for neutron-counting intensity during 4.5 ms are described. The systems are tested at Tien Shan ionization-neutron calorimeter INCA-54.

Introduction

Elaboration of the multipurpose astrophysical orbital observatory (MAOO) INCA based on ionization-neutron calorimetry is continued. The MAOO is designed (a) to study the PCR charge composition and energy spectra up to the "knee" energies ($10^{15} - 10^{16}$ eV) and spectra of high-energy electrons and diffusive gamma-rays up to 10^{13} eV; (b) to search for γ-ray discrete sources and dark matter signatures up to TeV energies; (c) to study interactions of high-energy particles. General features and potentialities of the instrument are described in [1] and [2], respectively.

Such a versatile device requires a corresponding recording system. It must, in particular, (a) record signals from scintillators in two modes of operation (fast one for detection of cascade and long-duration one for neutron counting); (b) have a multichannel analog-to-digital conversion system with a wide dynamical range (10^6) and a time $\tau_{\rm con}$ of recording into the fixed memory being independent of channel number; (c) record "Helium-2" gas neutron-counter signals as well as a time scanning system for neutron-counting intensity during 4.5 ms.

To determine the charge of primary cosmic-ray particles, a new-generation semiconductor coordinate-sensitive detectors of radiation particles are elaborated by means of the International Science and Technology Center. The detectors are to have better time (10 ns) and coordinate (20 m) resolution as compared with traditional microstrip detectors used in recent space experiments.

The real space instrument will have 16525 channels [1]. Elaboration of high-reliability system of amplitude analysis with such wide dynamical range (10^6) for this large number of channels is a very difficult problem. This work proposes a conceptual solution of this problem. At present, we test this approach by developing the Tien Shan ionization-neutron calorimeter INCA-54. Some results are described below.

At the present time the possibility of making of the MAOO and launching into 400-450 circular orbit is considered by the M.V.Khrunichev State Research and Production Space Center (*Khrunichev* Center) [4]. The instrument is proposed to be launched by a heavy *Proton* carrier produced by the *Khrunichev* Center [4] and being potentially able to launch about 20-ton pay-load.

The basic design principles

Intensified by the amplifier, amplitudes of the pulses from the particle detectors are conversed into a digital form by a special multi-channel system of amplitude analysis built on the basis of AD7888 type elementary ADC chips [3]. The chips have 12-bit conversion accuracy and a operation speed of 125 kSPS. Eight in-built separate channels are integrated in a single chip. Overlapping of the necessary dynamical range of input amplitudes ($\sim 0.5 - 1.5 \cdot 10^6$) by the 2^{12}-wide converters is achieved by using pairs of ADC channels for operation with the signals from the same detector (with different amplification coefficients of input signal in both the channels).

Nevertheless, if the total number of input channels is $\sim (2-3) \cdot 10^3$, the sequential principle of analogue-to-digital (AD) conversion implemented in AD7888 chips presents some drawbacks. Indeed, 16 elementary tact pulses being necessary for a single conversion and operation of 3000 input amplitudes done in turn would take ~ 50 ms, even if a 1 MHz system-timing clock will be used. This value is too large to provide an appropriate the whole instrument's dead time and to avoid growing difficulties with undistorted keeping of the remembered peak levels of pulse amplitudes on the inputs of ADC system during all this time. Luckily, the total duration of conversion time may be effectively reduced by splitting the whole amount of conversion channels into a number of hierarchically organized parts which could be operating in parallel.

As a base for building the hierarchically-subdivided ADC system, we use the standard CAMAC crates. The AD7888 ADC chips are mounted in the standard single-width CAMAC modules, 16 chips (128 operation channels) per module. Each chip having 8 in-built channels of AD conversion. A single 25-station CAMAC crate may hold up to 22 separate ADC modules, i.e. up to 2816 input channels. The remaining 3 stations of the crate are occupied by the two modules of system control: a double-width common-purpose crate-controller for the coupling of the whole crate with computer and a specialized single-width controller module destined for elaboration of the control signals and command sequences especially for ADC system.

Due to the distribution of ADC elements over a multitude of separate modules (each of which implements a functionally completed 128-channel AD conversion device) the whole operation time of the system may be drastically reduced, because all 22 modules of the crate are operating simultaneously during the amplitude measurements. 16 chips placed inside each module are divided into two groups (the "even" and "odd"); the chips of each group being operating in parallel too. Hence, the whole conversion cycle takes $16 \cdot 8 \cdot 2 = 256$ tact pulses that corresponds to $\tau_{\rm con} \sim 512$ μs with a 0.5 MHz frequency of synchronization clock. Here "16" is the number of tact pulses being necessary for a single conversion cycle, "8" is the number of ADC channels per chip (the channels being operating one by one, the channels with the same numbers simultaneously in the chips of "even" and "odd" groups) and "2" corresponds to the two groups of chips which are also operating one after the other.

The functional completeness of the each ADC module ensures a good scalability of the whole system, i.e., increase in number of modules installed in a crate.

Control of the ADC system

The multi-channel ADC system can work in the two operation modes: the measurement mode and the mode of data output. The measurements are

initiated by an external pulse signal — the trigger, which is elaborated by the special scheme in the moments, when something interesting is happening in the vicinity of experimental installation. The measurement phase lasts during the abovementioned operation time 512 μs; after it has been completed, the system locks itself and signals to the computer about it's readiness for the output of the fresh measurements data. The data output phase is initiated by computer which operates under the control of data recording program. After the data are rewritten to the computer's memory, the latter unlocks the ADC system by a special command.x'

The simplified circuit diagram of a 128-channel ADC module is shown in the Fig. 1. The 16 ADC chips are divided by pairs in the two groups — the "even" and "odd", the outputs of the chips belonging to the same pair being connected with each other and with the one of eight data pins of the chip of local random access memory (RAM). The latter, having organization 256x8 bits, is destined to save the sequential amplitude codes elaborated by ADC chips during the measurements (16 sequential bits per each input channel, 8 channels per each ADC chip and two chips connected to data line; totally 256 bits per each line of data). The sequential data codes are kept inside the local RAM chips until they would be read by the control computer (the final unpack of the data corresponding to each input channel and calculation of binary amplitude codes according to sequential ones proceeds in the data output phase under the program control).

In the measurement phase all the eight ADC chips belonging to each of the "even" and "odd" groups are operating simultaneously, in parallel. Also, all the ADC modules placed in the system crate are operating in parallel too. This circumstance ensures a reasonably confined duration of the total operation time.

The simultaneous operation of independent ADC modules is supported by synchronization signals being generated by the controller module of ADC system and transmitted via the *W* lines of the CAMAC crate bus.

First of all, the controller module generates the basic tact sequence with the period of 2 μs (the beginning of this sequence is synchronized with the arrival moment of external trigger). Tact pulses are transmitted to ADC chips through the line *W12* and synchronize the process of AD conversion. At the each time moment only a single ADC chip may be operating (and using the lines of data bus) in the each chips pair — either the "even" or the "odd" one; their operation order is defined by the levels (low or high) at the *W10* line of CAMAC bus. The 8-bit words of input commands which are necessary for AD7888 type chips (the contents of these commands defines, in particular, the number of input ADC channel currently being under operation) are generated by controller module and transmitted sequentially through the line *W11*.

Data sequences elaborated by ADC chips and carrying the information about the voltage levels at the inputs of ADC channels are remembered in the local RAM storage ("as is", 16 separate conversion results in sequential code one after another for the each *Data* line). The system controller generates all the necessary for the RAM chip operation signals: the binary code of the current RAM address (transmitted through the lines *W17-W24*), the pulses *Chip Select* (the line *W9*) and *W/R* (the line *W16*). The current status of voltage levels at the *Data* pins of RAM chip is remembered in the moments of rising edge of the signal *W/R*.

The data output mode

Completion of the measurement phase and the readiness of ADC system for data output are signalled through the active (low) level at the CAMAC line *Q* in return to the command *F8* addressed to the ADC system controller.

In the phase of data output the operation order of ADC channels and the time duration of the whole process are defined by the program of the external computer. The specialized ADC system controller remains in the locked state and the data exchange proceeds through the common-purpose crate-controller module connected to the parallel port of recording computer. (Crate-controllers of such a kind so as the corresponding program drivers are especially designed and widely used at the Tien Shan station in extensive air shower experiments). By the means of crate-controller the recording program sets the necessary codes of the internal RAM address on the lines *W17-W24*. Selection of the RAM chip in a particular

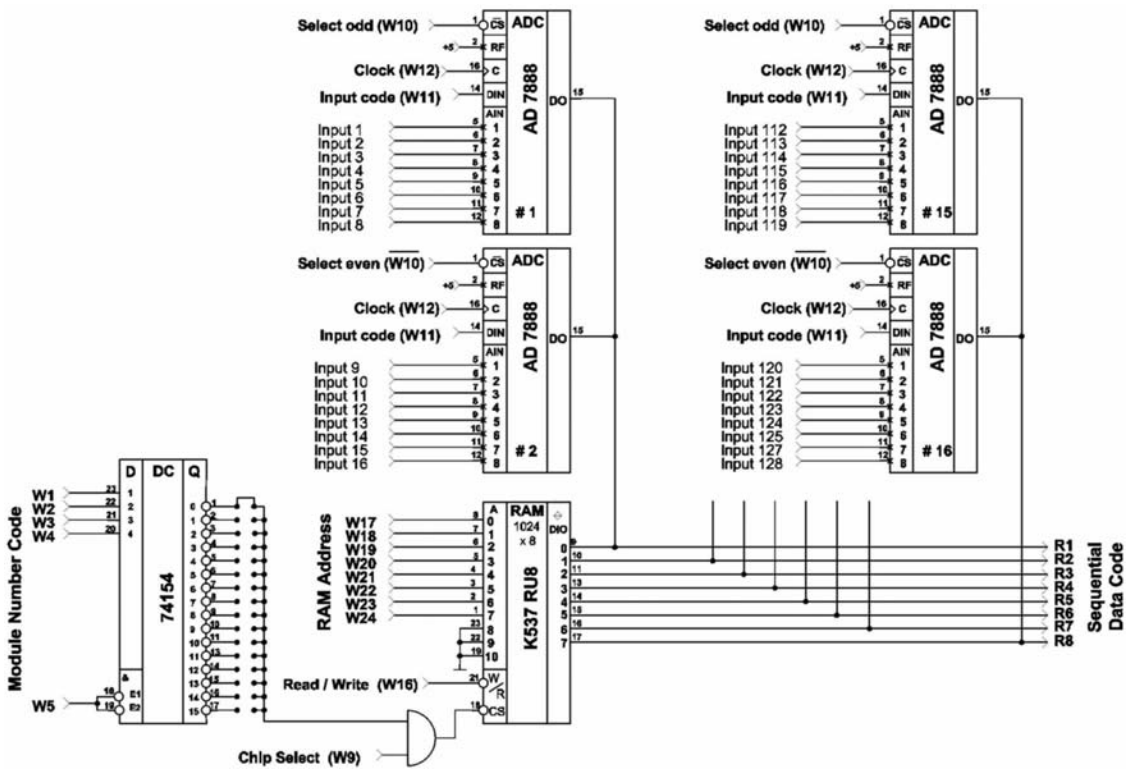

Figure 1: The simplified schematic diagram of the AD conversion module.

ADC module is secured by the module number decoders placed inside each module. Decoders accept the binary code of module number from the lines *W1-W8* (were the code is pre-set by recording program through the crate-controller registers) and their output levels are used as *Chip Select* signals for connection the data outputs of a selected RAM chip to the *R* lines of the CAMAC crate bus (only a single RAM chip may be connected to the bus at the each particular moment). Information from the *R* lines is read through the crate-controller by the control program.

After the reading of data is completed, the recording program unlocks the ADC system controller by using a special CAMAC command (*F9*).

It should be emphasized that the real space instrument will use modern microcontroller system (instead of CAMAC) compatible with on-board computers. However, the above-described solution of the system architecture will be invariable.

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