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The Flight Electronics System for the Cosmic Ray Electron Synchrotron Telescope (CREST) Experiment

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Abstract: The balloon-borne Cosmic Ray Electron Synchrotron Telescope (CREST) experiment will employ a novel distributed electronics system to collect timing and pulse height information from 1024 BaF_2 crystal detectors and 42 PMTs in its anticoincidence shield. The timing of single photoelectron triggers from the PMTs in the crystal array is recorded to an accuracy of 1 ns least count. Wide dynamic range pulse height information from two dynodes on each PMT is recorded when two or more crystals receive single photoelectron triggers. Timing and pulse height information from the anticoincidence shield is recorded only when received within a preset time window of crystal array triggers. Integral Cockroft-Walton high voltage power supplies, potted within the PMTs are individually set by a digitally addressable control and monitoring system. Extensive use of FPGAs and CPLDs enable high-speed synchronous operation and low power consumption with a flexible distributed and modular architecture.

Introduction

CREST is a long duration Antarctic balloon experiment that will measure multi-TeV electrons in the galactic cosmic rays. The energy spectrum of these electrons will help identify local acceleration sources and mechanisms within or galaxy. High-energy electrons will be detected by synchrotron radiation emitted by primary electrons in the Earth's magnetic field. A fraction of this radiation, intercepted by an array of BaF_2 crystals, will be used to determine the energy and possibly charge sign of the primary electron. A detailed description of the science objectives and instrumentation for CREST [1] can be found in these proceedings. The electronics design presented here has been greatly influenced by extensive simulations of the CREST instrument [2]. The primary function of the CREST electronics system, shown schematically in Fig. 1, is to record timing and pulse height information from the 1024 BaF_2 detectors and the 21 veto scintillators. Additionally it is responsible for control and monitoring of PMT voltages, system calibration via a LED calibration pulser, threshold setting, acquisition of housekeeping data (rates, currents, voltages, temperatures, etc.) and control of data storage and telemetry packaging. The design of the CREST electronics balances the various and often competing demands of high speed, low power consumption, large dynamic range, failure tolerance, distributed placement of detectors and near vacuum operation. We have designed a triggerless, modular and distributed system that makes extensive use of Clocked Programmable Logic Devices (CPLDs) to provide local high speed timing, Field Programmable Gate Arrays (FPGAs) to perform sophisticated high speed local decisions and Bussed Low Voltage Differential Signaling (BLVDS) to connect and synchronize widely separated modules and reduce the need for extensive cabling. Modularity is achieved by dividing the BaF_2 crystal array into

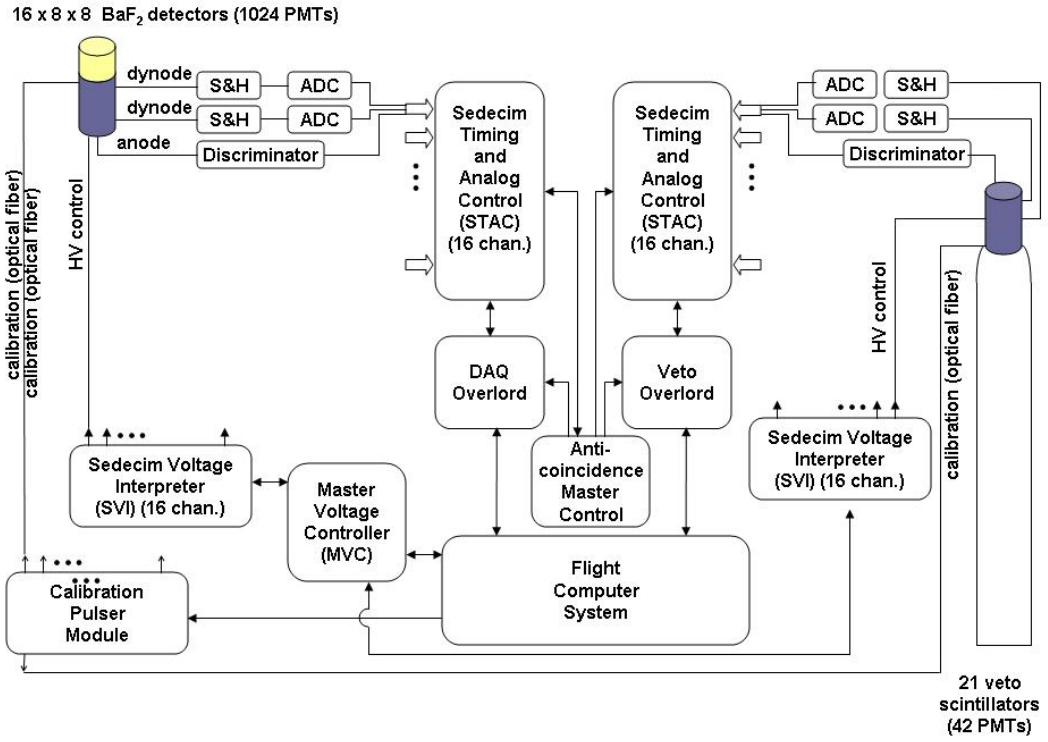

Figure 1: Block diagram of the overall CREST electronics.

eight planks, each consisting of eight Sedecim (16) PMT modules.

PMT Control/Monitoring

Operation in a near vacuum requires the high voltage portions of the PMTs to be isolated and potted. To facilitate this, a Cockroft Walton (CW) power supply is potted into the base of each PMT. This CW power supply is individually controlled by a precision 0-2V control voltage with a 1:1000 gain. A Sedecim Voltage Interpreter (SVI) has been designed and fabricated so that it performs the control and monitoring function for a module of 16 PMTs. Under programmable control of a Master Voltage Controller (MVC), the SVI provides individual control voltage setting, control voltage read-back, high voltage supply monitoring and current monitoring for each PMT. Each CW base is powered by an isolated 5V supply. A bi-directional (redundant) common SPI serial interface with parallel addressing is used to control and monitor all 8 SVI boards in a plank. Each SVI board provides its own internal diagnostics and generates an alert when any PMT draws excessive current and also when any PMT supply voltage drops by more than 10%.

Analog Signal Processing

The anode signal from each PMT is first sent to a 16-channel discriminator board. To obtain sub-ns timing, digital potentiometers provide individual discriminator thresholds corresponding to the ~0.5 pe level. These individual thresholds are read back by ADCs. A threshold setting mode controlled by the flight computer can systematically adjust the individual PMT thresholds while monitoring trigger rates.

In order to measure the large dynamic range (20 keV - 20 MeV) in deposited energy that will be seen in the BaF_2 crystals, two dynode taps (DY#7 and DY #10) are provided by each PMT. These

positive going dynode signals are captured by a Viking Analog (VA) board that contains two 34 channel VA32-HDR11 ASICS. Each channel consists of a charge sensitive amplifier, shaping amplifier, peak sensing sample and hold and an analog multiplexer. Thirty-two of the 64 channels are used for the dynode signals, four are used for baseline monitoring and one is for readout of the signal from a photodiode used to monitor the output of the LED-based Calibration Pulser Module. The remaining channels are not enabled. The bias voltages for each VA ASIC are individually adjustable and are digitized for monitoring on the VA board.

Timing

A Sedecim Timing and Analog Control (STAC) board controls the discriminator board and the VA board. The STAC board digitizes (12 bits, 20Msps) the signal from each VA channel and provides 1 ns least count timing for each discriminated anode signal. In addition, it provides clean biases for the discriminator and VA boards, temperature monitoring and current monitoring for each internal power rail.

1 GHz timing precision is achieved by using four CPLDs running at 250 MHz, successively phase shifted by 90° (See Fig. 2). Timing accuracy is assured in three ways: across the CPLDs by design, within the FPGA by careful I/O selection and by tightly controlled board trace lengths. A FPGA examines the output of the CPLDs and reconstructs the discriminated rising edge to a precision of 1ns. The time determined in this way is transmitted through a delay pipe then stored in Block Ram within the FPGA. In an early stage of the reconstruction these signals are also examined to determine the number of coincident PMT signals within overlapping 32ns windows inside each STAC board. Two output signals (≥ 1PMT and ≥ 2 PMT) derived from this examination are sent to an external Anti-coincidence FPGA. A system-wide "digitize" signal is derived from this collection of incoming signals and transmitted back to all STAC boards and to the dual Overlord cards (see below). This signal, in coincidence

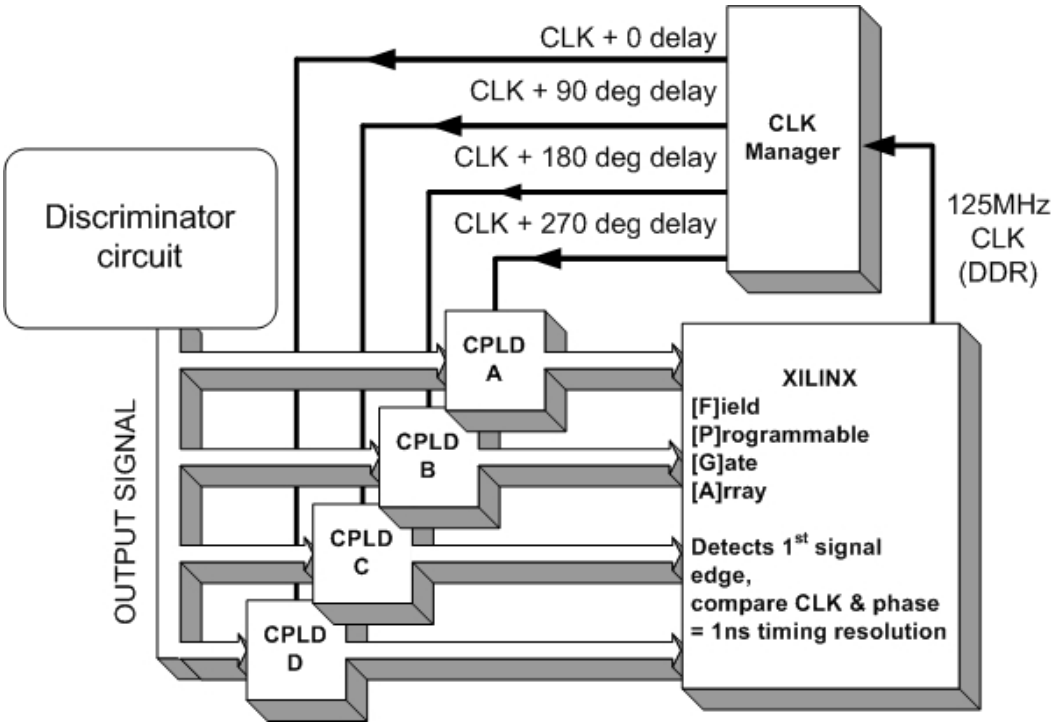

Figure 2: Phased clock reconstruction provides 1ns timing resolution

with the times emerging from the delay pipe, will only then initiate digitization of the dynode signals from each PMT. This allows a significant reduction in data storage. Furthermore only PMT signals exceeding threshold are digitized and stored. The times and digitized dynode signals are then transmitted to a central Overlord board where they are sorted and stored.

An identical chain of electronics with minor modifications is used for the Veto system. The high rates (~ 50 kHz) from each veto PMT require that not all STAC board channels will be populated. The large physical separation between veto PMTs also makes this a more practical solution. Coincidence count signals from the Veto system are not transmitted to the Anti-coincidence Master, but the returning "digitize" signal is used as above to initiate readout of the dynode outputs associated with veto paddles.

Control, Data Collection, Calibration

Commercial FPGA interface boards (Opal Kelly XEM3010) are used to collect data from and control the local electronics described above. Three such interface boards are employed: a DAQ Overlord controls the STAC boards associated with the BaF_2 array, a Veto Overlord controls the STAC boards associated with the veto counters, and a Master Voltage Controller (MVC) controls the SVI boards. These all reside on an XEM Carrier board which also contains circuitry that performs the anti-coincidence decision (Anti-coincidence Master Control in Fig. 1) required to reject veto data arriving outside an adjustable time window surrounding two or more hits in the BaF_2 array. This results in a dramatic reduction in extraneous veto data volume while preserving veto information that could be associated with signals in the BaF_2 crystal array. Note that the veto decision is not used in any prompt hardware anti-coincidence. All the resulting data is stored and is available for later analysis. A second, identical XEM Carrier board provides redundancy in case of failure. The Calibration Pulser Module generates a calibration light pulse for each PMT. Optical fibers of matched length distribute this signal to all PMTs and to photodiodes on each VA board. The resulting data provide relative time offsets for each channel, which are used to calibrate and correct the timing data. The photodiode signals are used to monitor the overall light output of the pulser and correct the ADC data.

Flight Computer

At the heart of the flight computer system is a Pentium–M class single board computer with USB interfaced flash memory data storage. The flight computer is the top-level control for all the electronics described above. It initiates the calibration pulse and uses the calibration data that it receives via the DAQ Overlord to determine the time offsets. The flight computer adjusts the discriminator thresholds during calibration mode by monitoring the PMT rates as individual thresholds on the discriminator boards are systematically lowered. During regular data taking, the DAQ and Veto Overlord are polled for event data and those data are then formatted and stored on the flash memory. Through the MVC interface it sets and monitors the PMT voltages and currents; it sends telemetry data through a PCM encoder (implemented via an Opal Kelly XEM3010) to the Consolidated Instrument Package (CIP) and receives ground control data via the CIP. It collects housekeeping data from all the electronics boards as well as environmental sensors and incorporates these into the data stream.

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