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The VERITAS Digital Asynchronous Transceiver

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Abstract: The VERITAS array-level trigger requires a simultaneous coincidence between multiple telescopes to initiate the readout of data and is essential to reducing the overwhelming background of local muons whilst efficiently recording light from VHE gamma-ray initiated air showers. The selection of coincident events in hardware reduces the overall trigger rate allowing the individual telescopes to trigger at lower thresholds, decreasing the energy threshold of the system. Short asynchronous pulses, serial event-numbers and long status flags must be distributed between telescopes. Coaxial cable cannot be utilised over the required distances and a serial, sequentially implemented, distribution scheme is undesirable as the dead time of the trigger system must be kept to a minimum. Instead a Digital Asynchronous Transceiver (DAT) employing parallel optical link technology has been developed. Combinatorial logic functions are implemented in Xilinx Spartan-3 FPGAs providing a versatile solution capable of transmitting data asynchronously on each of 11 channels with nanosecond accuracy and incurring no dead-time. The laboratory performance and integration of the DAT modules into VERITAS are presented and the benefits and draw-backs of this novel approach discussed.

Introduction

VERITAS consists of four 12 m diameter atmospheric Čerenkov telescopes equipped with photomultiplier cameras [1]. The array uses a multilevel trigger system to reject fluctuations in background light whilst efficiently recording signals from gamma-ray initiated air showers [2] requiring the distribution of multiple, fast, digital pulses between telescopes. A versatile solution is essential as variable width event numbers and long calibration flags must also be transmitted. The data from each VERITAS camera pixel is digitised into 2 ns slices by custom built 500 MHz FADC boards [3]. Upon receiving an array trigger signal the FADC buffers are read out. The trigger signals require nanosecond accuracy to readout the FADC modules from the correct point in the buffers. The FADC readout time has a direct effect on the telescope deadtime and energy threshold, so it is important the minimise the readout window around the data pulse (typically 48 ns). Accordingly the Digital Asynchronous Transceiver (DAT) modules have been developed at the University of Leeds in collaboration with Hytec Electronics Ltd. The modules are linked by fibre optic interconnects running between telescopes.

Implementation

The DAT consists of two, 6U high, single width VME modules denoted DAT-TX and DAT-RX, transmitter and receiver respectively, Figure 1. Control and monitoring takes place via a VME interface embedded into an onboard Xilinx Spartan 3 XC3S50 Field Programmable Gate Array (FPGA). To maintain signal integrity and avoid any lightning induced power surges a 62.5/125 μm core fibre optic interconnect is used to transport signals over the distance of around 150 m between telescopes. The conversion of electrical signals to optical signals is achieved using the Infineon 1.25 Gbit/s parallel optical link (PAROLI 2®) consisting of a 12 channel, 850 nm VCSEL driven transmitter and PIN diode-array receiver. As a matter of laser safety a given PAROLI channel will become disabled if a signal exceeds a duty cycle

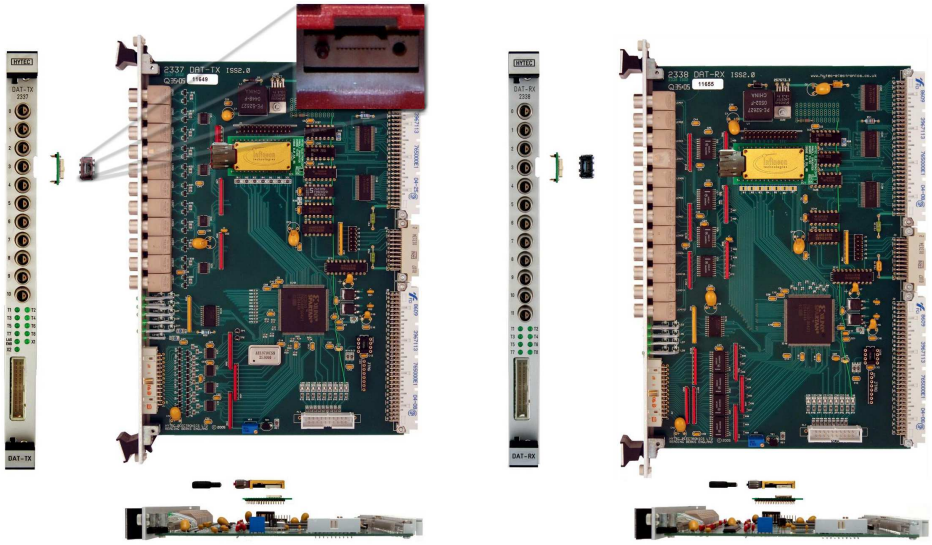

Figure 1: The DAT transmitter (left) and receiver (right) with a close up of the Infineon PAROLI (inset).

(DC%) of 57% within 1 μs. The asynchronous variable width input data signals *cannot* be sent to the PAROLI directly, they must first be modulated to this DC% requirement in a recoverable manner. This is achieved by encoding incoming data signals with a 25 MHz clock through exclusive OR (XOR) gates at the transmitter. The encoded data signals and a copy of the clock are optically transmitted to the receiver where a second set of XOR gates recovers the data. Using this asynchronous, combinatorial method deadtime incursions associated with sequential logic are avoided. Combinatorial logic is usually implemented in surface mounted IC chips. To accommodate rapid design change and the future possibility of a PAROLI without rigorous duty cycle constraints, all logic is performed within the onboard FPGA. As the gate array is used to implement the VME interface this is an economical solution.

FPGA Combinatorial Encoding

At the transmitter 22 differential signals from twinaxial and IDC inputs are buffered onto the FPGA. A 25 MHz clock is input via a dedicated clock-buffer to a low skew network on the FPGA and fanned out 12 times. Each of the fanned out clocks

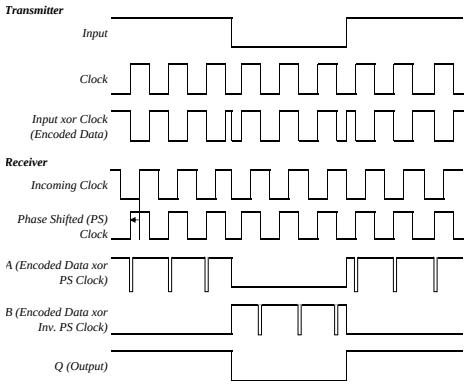

Figure 2: Depiction of XOR encoding embedded in the DAT FPGAs.

enters an XOR gate with a corresponding data line, except for the twelfth clock, which enters an XOR gate with ground to maintain duty cycle and transit time. The signals are buffered to differential outputs on the FPGA. During laboratory tests the duty cycle of the encoded transmitter output was seen to vary by around 0.5% (200 ps) from a low input data state to a high input data state. This duty cycle dependence on the high/low state of the input is attributed to rising and falling signal edges tak-

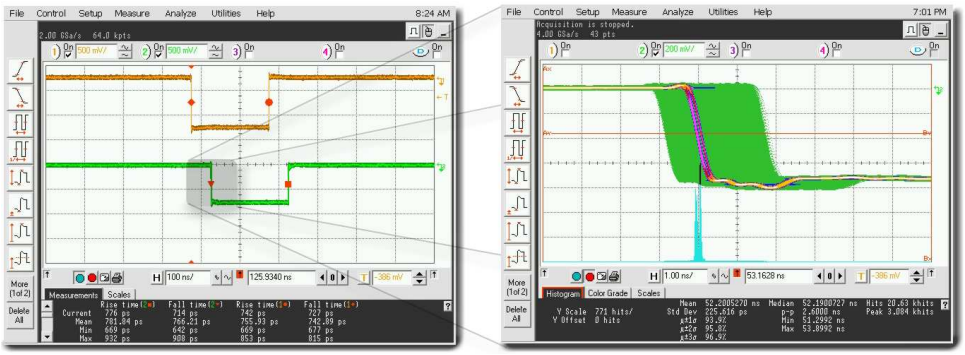

Figure 3: Measurement of the arrival time of the falling edge of the DAT output relative to a reference pulse (upper trace) for a single channel.

ing different paths through the FPGA, leading to unequal transition times.

At the receiver the differential clock is buffered to a digital clock manager (DCM). Feedback into the DCM facilitates a phase shift between the input and output with a resolution of 156 ps. The phase shifted clock is fanned out and entered along with the 11 data lines to XOR gates. Due to the duty cycle dependence on the high/low state of the input it is not possible to phase shift the clock to a point where the input is accurately reproduced for both high and low input states. Instead the clock is phase shifted to a position where the output accurately represents the input during a low state. During a high state the output shows sharp spikes down to the low state. Thus for transmitter input as shown in Figure 2 the result *A* is obtained. To remedy this, an inverted copy of the phase shifted clock is XOR combined with a second copy of the data to produce the result *B*. The results *A* and *B* are used to clock a dual data rate flip-flop at the output stage to reproduce the data, *Q*. The flip-flop output *Q* is set high by a rising edge on input *A* and low by a rising edge on input *B*. The output is not sensitive to falling edges on either input.

Performance

To characterise the performance of the DAT modules the arrival time of the falling edge of a periodic, 1 MHz, 200 ns wide input to the transmitter is measured at the receiver output, relative to the falling edge of a reference pulse as shown in Figure 3. The channel-to-channel skew and average jitter over all channels are taken as the two key indicators of performance. The jitter on each channel is obtained from the distribution of around 20 k measurements over a 2 m long, MPO terminated, 12 channel fibre ribbon cable. The total jitter is a combination of two principle components: random jitter, R_J, and deterministic jitter, D_J. Random jitter is uncorrelated and unbounded and is measured in terms of the standard deviation, σ_{R_J}. Random jitter is always Gaussian and for a given bit error rate, BER, is related to the quantity Q, a multiple of the standard deviation of the Gaussian, by $R_J = 2Q\sigma_{R_J}$. Deterministic jitter is bounded and represented by a peak-to-peak value. The total jitter, T_J for a given BER is given by the summation of R_J and D_J. The deterministic and random jitter may be separated from the recorded distribution via the dual-Dirac model and used to predict a total jitter for the industry standard BER of 10^{-12} (which corresponds to $Q = 7$). In the dual-Dirac method the recorded distribution is modelled by two delta functions displaced in time and convolved with a Gaussian. σ_{R_J} is then estimated by fitting the outer edges of the measured jitter distribution. The displacement of the delta functions is given by the separation of the outer peaks in the measured distribution and is taken to be D_J. A total jitter of 2.50 ns (or $\pm$1.25 ns) peak-to-peak for a BER of 10^{-12} is obtained for the channel in the example distribution shown in Figure 3. The measurements for all channels over a 60 m cable are

Channel	T_{ar} (ns)	PP_{ar} (ns)	RMS_{Ar} (ns)	HITS $(kHits)$	σ_{R_J} (ns)	R_J (ns)	D_J (ns)	T_J (ns)	95% (ns)
0	346.00	2.47	0.22	20.49	0.03	0.47	2.22	2.69	1.02
1	344.84	1.55	0.10	20.28	0.05	0.73	1.15	1.88	0.25
2	344.45	1.80	0.16	20.52	0.03	0.50	1.53	2.03	0.40
3	344.98	1.73	0.15	20.17	0.05	0.67	1.36	2.03	0.40
4	345.71	1.73	0.13	24.59	0.03	0.41	1.50	1.91	0.40
5	345.44	1.58	0.12	20.86	0.04	0.56	1.28	1.84	0.35
6	345.48	1.78	0.16	20.02	0.04	0.55	1.48	2.03	0.47
7	345.30	2.02	0.15	20.74	0.03	0.50	1.75	2.24	0.51
8	345.10	1.96	0.17	20.12	0.02	0.35	1.78	2.12	0.69
9	345.60	3.13	0.30	20.97	0.10	1.44	2.34	3.78	1.44
10	345.14	1.82	0.12	20.41	0.03	0.44	1.58	2.02	0.36

Table 1: Arrival time statistics for all 11 data channels of the first DAT pair over 60 m of fibre. Where T_{ar} is the average arrival time and PP_{ar} and RMS_{ar} are the peak-to-peak and RMS values of the recorded distribution. σ_{R_J}, R_J, D_J and T_J are the determined standard deviation, random jitter, deterministic jitter, and total jitter.

shown in Table 3 and an average total jitter of 2.20 ns (or $\pm$1.10 ns) is obtained. This BER extrapolation to 10^{12} pulses is not intended as a replacement for measurements made on a dedicated BER machine but simply provides a quick estimation of the worst case jitter. A more practical estimate of the jitter, in the absence of a Gaussian distribution, that will effect the trigger chain on an event-by-event basis is simply the time over which 95% of pulses arrive. On average over all channels, 95% of pulses arrive within 0.570 ns (or $\pm$0.265 ns) of the average for that channel. The skew between output channels from the average arrival times is 1.6 ± 0.4 ns (at the 95% confidence level). Since the system introduces no deadtime the minimum pulse width that can accurately be transmitted is only limited by the signal switching speed and the system jitter. The minimum transmittable pulse width is around 5 ns. This is also the time gap required between consecutive pulses, and therefore the maximum transmittable data rate is 200 MHz.

Critical Evaluation

Eight DAT pairs are installed and working on VERITAS. However, the FPGA code and methodology have proven complicated due to the accuracy required to align the clock with encoded data at the receiver. If the alignment is not correct at the subnanosecond level a given channel will produce spurious noise at either the clock frequency (25 MHz) or double the clock frequency (50 MHz). These pulses have a width corresponding directly to the misalignment of the clock and encoded data signal and a minimum width of around 2 ns, the signal switching time at the FPGA output stage. Spurious pulses do not occur at all if a channel is aligned. In practice a fibre-ribbon cable must be used to connect the DAT modules to ensure that the 12 fibres are of identical length.

Acknowledgements

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