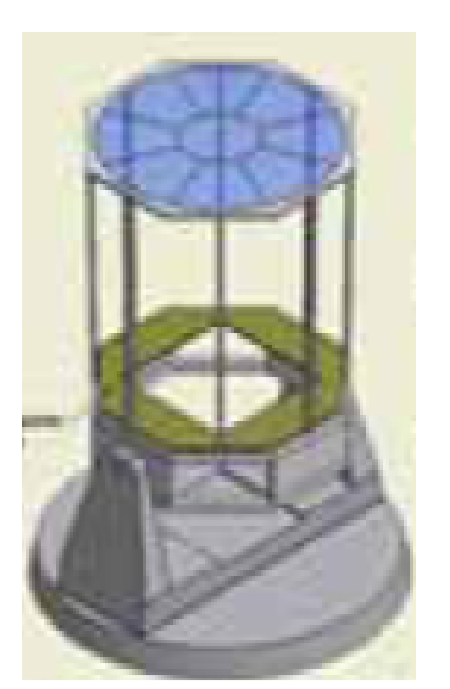




# Gamma Air Watch (GAW): the electronics and trigger concept

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The new approach of GAW for the detection of gamma rays imposes specific requirements on the electronics design.

## Electronics main characteristics:

- $\sim 10^5$  pixels
- Single Photon Counting
- free running data-taking
- 100 MHz acquisition rate
- trigger based on the number of active pixels

## Focal Surface Detector:

- array of MAPMTs
- Modular Front-End electronics (FEBrick)
- Backplane
- Modular DAQ (ProDacq)
- Mainboard with trigger system

## MAPMT

(Hamamatsu R7600-03-M64):

- 64 anodes in  $8 \times 8$  matrix
- good quantum efficiency for  $\lambda > 300$  nm (max 20% @ 420 nm)
- gain  $\sim 3 \times 10^5$  for 0.8 kV voltage

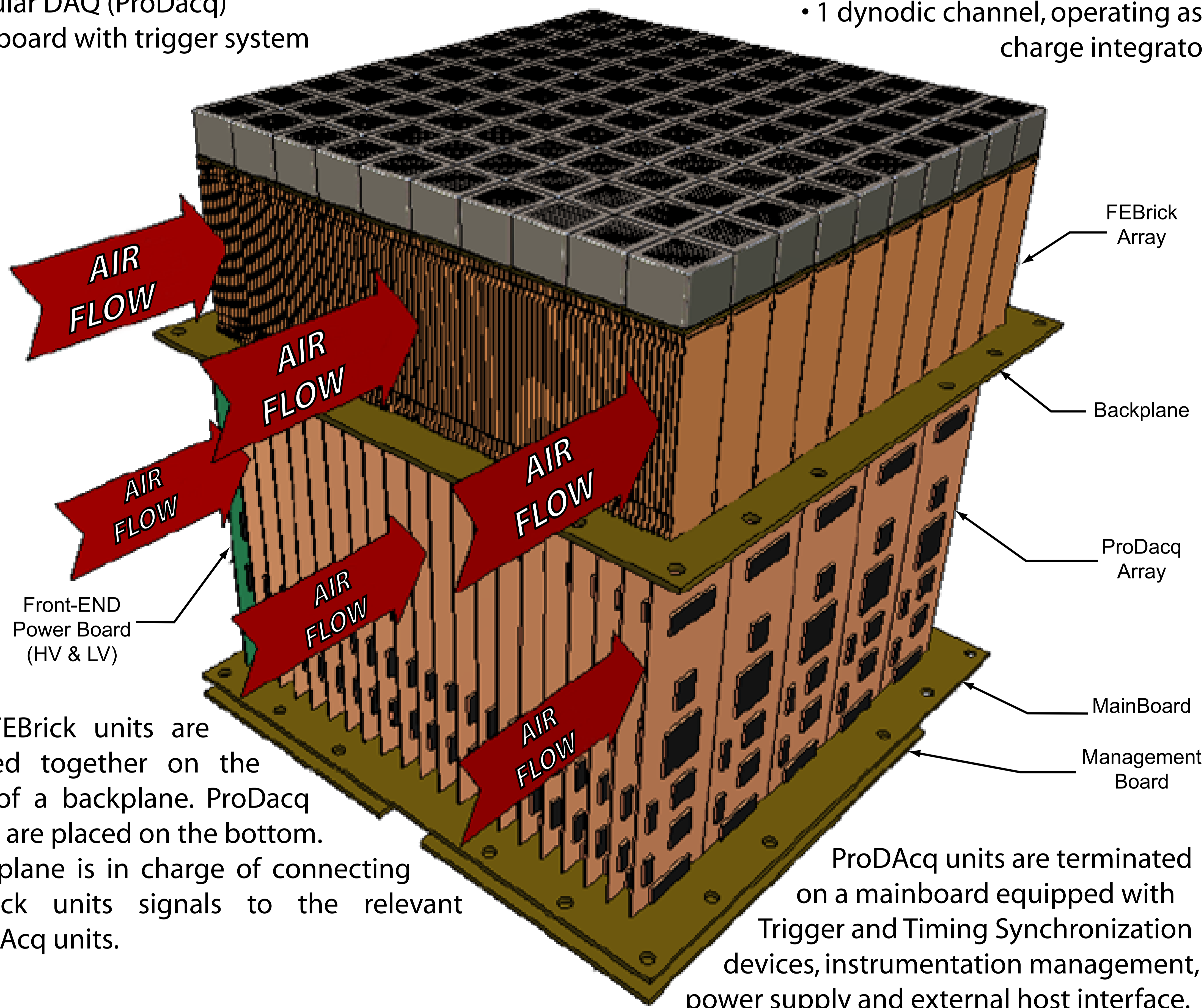
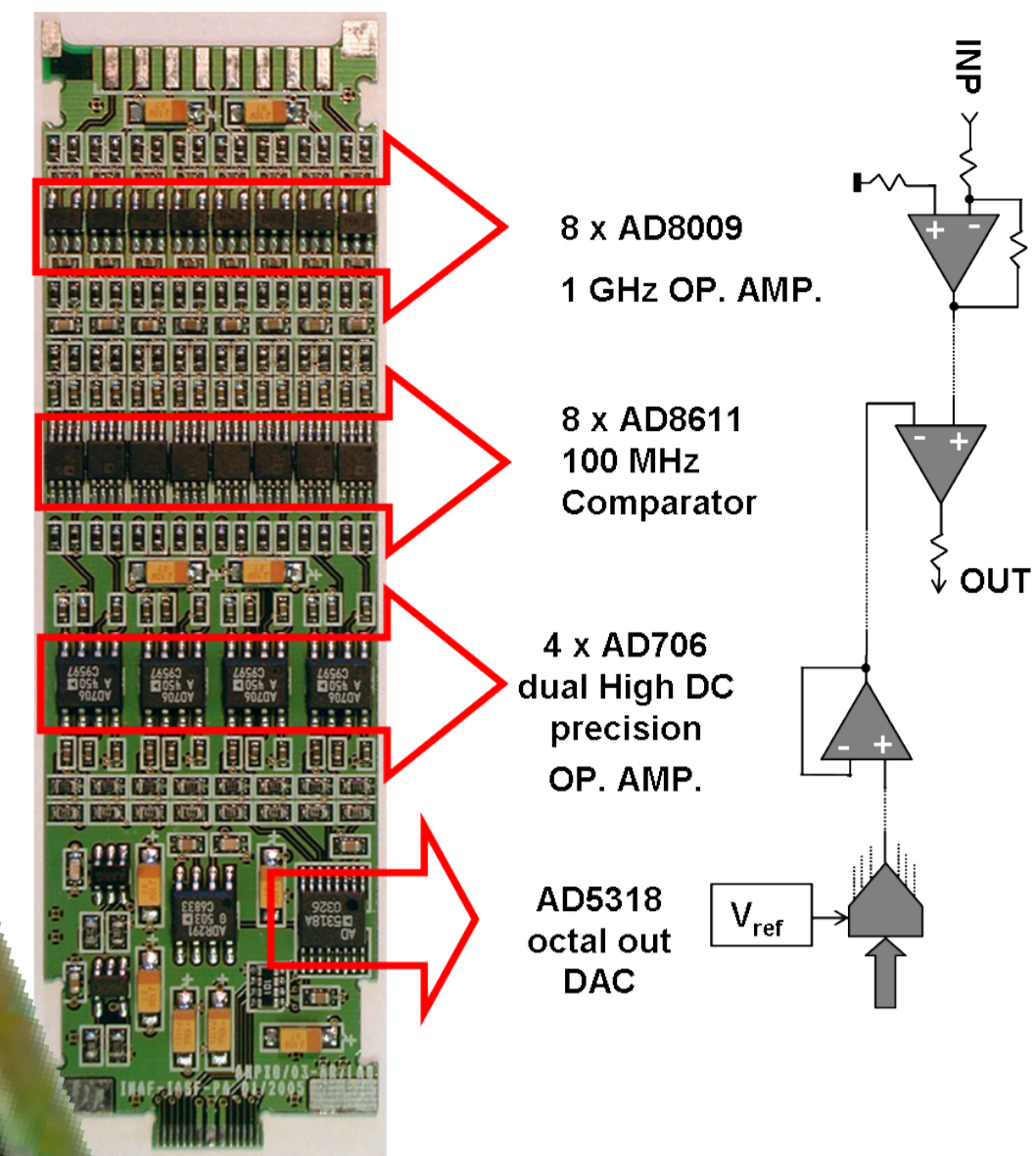
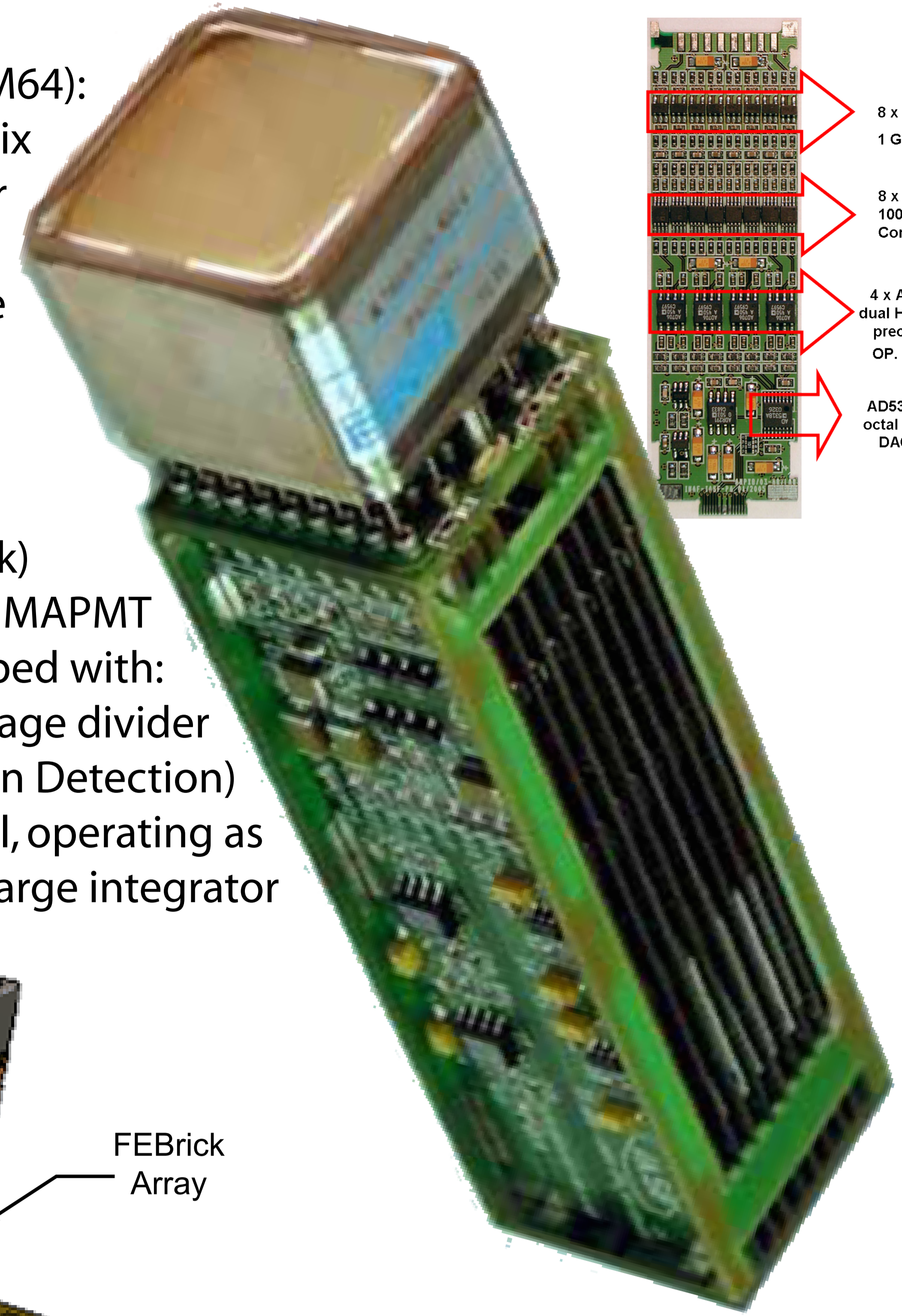
## FEBrick

(Front-End Brick)

processes signals from one MAPMT

FEBrick is equipped with:

- Low power active high voltage divider
- 64 anodic channels (Single Photon Detection)
- 1 dynodic channel, operating as charge integrator



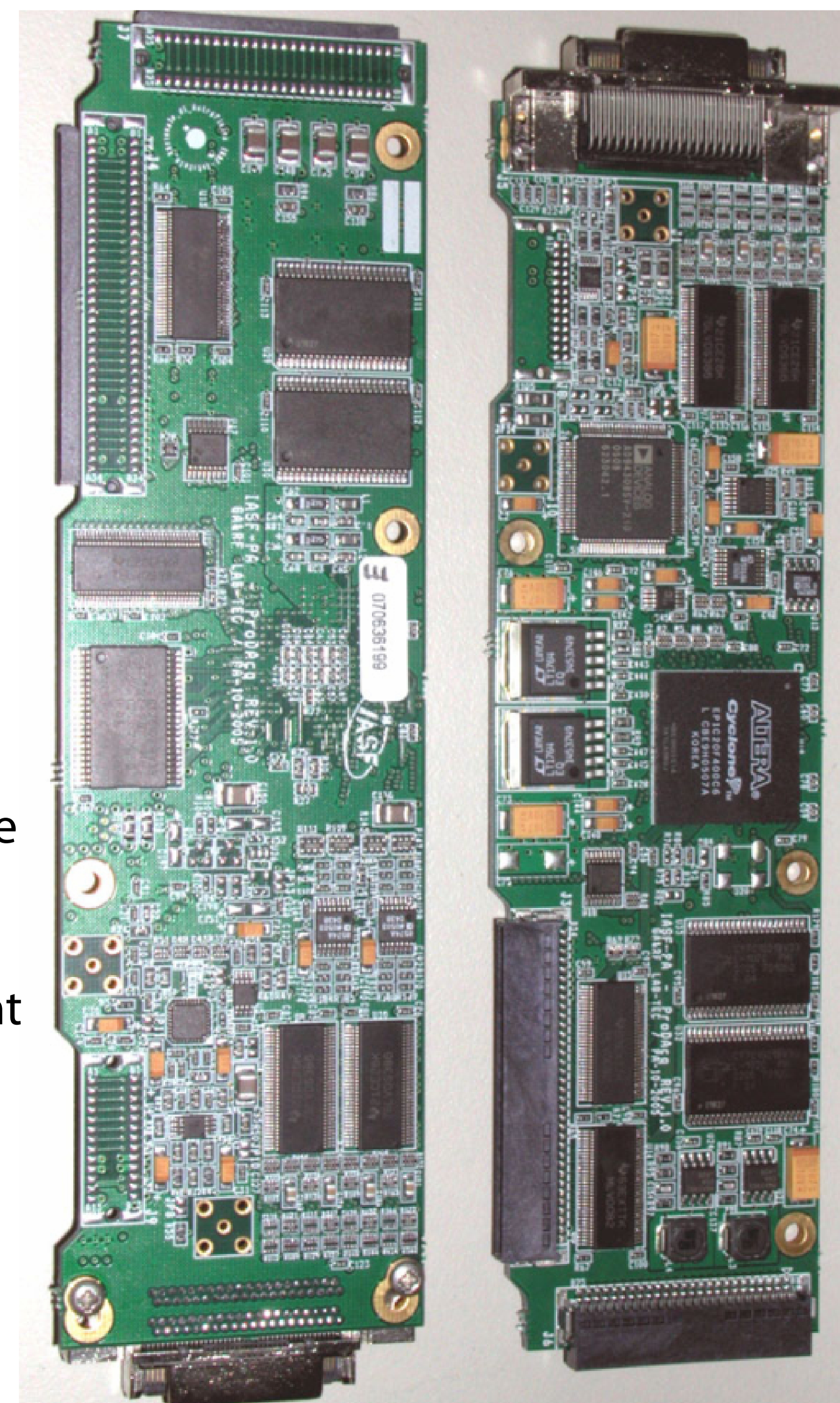
All FEBrick units are placed together on the top of a backplane. ProDacq units are placed on the bottom. Backplane is in charge of connecting FEBrick units signals to the relevant ProDacq units.

ProDacq units are terminated on a mainboard equipped with Trigger and Timing Synchronization devices, instrumentation management, power supply and external host interface.

## ProDacq

(Programmable Data Acquisition)

- Managed by a reprogrammable FPGA
- Digital signals recorded in memory
- Input analogue signal sampled by ADCs
- Each ProDacq receives data from one FEBrick



## Trigger system

based on three trigger levels:

- 1<sup>st</sup>: fast discriminator on FEBrick = simple threshold on each pixel signal  $\rightarrow$  transformed in digital signals (Pixel-on)
- 2<sup>nd</sup>: the focal surface is searched, online, by FPGAs on the MainBoard for a given number of pixel-on inside all possible squares of  $2 \times 2$  PMTs.
- 3<sup>rd</sup>: validation of second level triggers. Decide the relevant

Each Mainboard FPGA receives data from one FEBrick. Each FPGA exchanges data with its neighbours. The trigger operates in a pipelined scheme and makes a decision each 10ns. Relevant data is then read from the internal memories

