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Sigma-Delta compensation of pedestals in the 1^{st} level surface detector trigger of the Pierre Auger Observatory

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Abstract: Large temperature variations such as generally observed in desert like environments as the Argentinian pampa can cause significant variations of ADC pedestals in the analog part of Front End Boards. This drift may affect the stability of trigger conditions especially when working at thresholds close to the FADC pedestals. To compensate for such effects and to keep the trigger conditions stable in the current design, a calibration channel constantly modifies the trigger thresholds in a slow loop. In this paper we suggest a trigger that is independent of the pedestal as a superior approach. The algorithm and its implementation in the FPGA firmware of the Front End cards are presented. Results obtained from operation in a climate chamber illustrate the pedestal drift in the 1^{st} level trigger and demonstrate the effect of the sigma-delta compensation. The algorithm is now being tested under real conditions in 7 test tanks.

Introduction

The surface detector of the Pierre Auger Observatory comprises 1600 water Cherenkov tanks placed on a triangular grid of 1.5 km baseline yielding a total area of 3000 km^2. The signals from each tank are read out by three 9-inch photomultipliers and the signals of the anodes and dynodes are continuously sampled in Front-End Boards at 40 MHz frequency by 10-bit AD9203 Flash ADCs. With 5 bits of overlap between the two ADCs of a PMT, an effective dynamic range of 15 bits is achieved, sufficient to allow for triggering on small signals and to not saturate for large particle densities near the core of extensive air showers. The outputs of the six ADCs are processed by Programmable Logic Devices (PLD) working as trigger/memory circuitry (TMC). The TMC evaluates the ADC outputs for interesting trigger patterns, stores the data in buffer memory, and informs the detector station micro-controller in case a trigger occurs. The station controller sends trigger packets and, when requested, event data to the observatory campus via a wireless network. Electric power at each tank is provided by solar panels and precise timing is obtained from a GPS clock. More details about the Pierre Auger Observatory can be found in Ref. [1].

The large ambient temperature variatios between day and night on short time scales and additional seasonal variations on larger time scales result in temperature variations in the electronic box, reaching often more than 50 degrees. As a result, this causes significant variations of the FADC pedestals of both the dynode and anode signals. A very low dependence of pedestal vs. temperature also occurs (see Figure 1), however it concerns a relatively small fractions of tanks. A typical example of a large pedestal variation for a single tank is depicted in Figure 2. The temperature changes cause variations by more than 5 ADC channels over full temperature range (see Figure 5). Thus, applying fixed trigger thresholds would significantly affect the trigger rate especially for the Time over Threshold (ToT) trigger which operates at thresholds (0.2 VEM $\approx$ 10 ADC-channels) that are relatively close to the pedestals. A drift of 5 ADC channels would correspond to 50 % of the trigger threshold. To achieve constant trigger conditions despite these changes, a calibration channel currently modifies the thresholds continously. However, keeping a stable pedestal rather than tuning

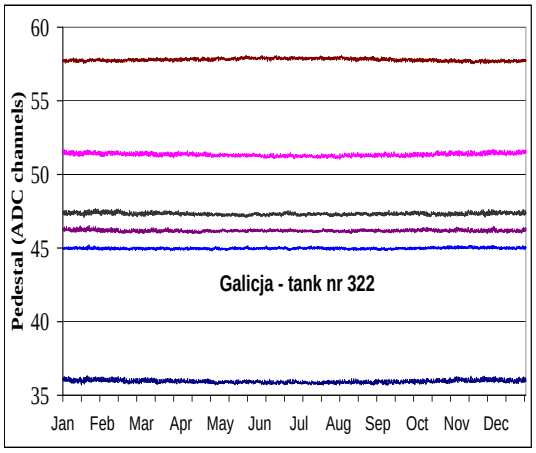

Figure 1: Pedestals as a function of time for all channels in the Galicja tank (No. 322) from Jan 1^{st} until Dec. 31^{th}, 2006. This tank contains the Front-End-Boards with an exeptional small variation of pedestals less than 0.67 ADC-channel in the most temperature-dependent channel.

the thresholds for a single tank via the slow calibration loop appears to be a better approach.

For this purpose, additional routines were introduced to compensate for the observed temperature drift of the pedestals.

The Sigma-Delta algorithm [2] has been proven very sucessful for such type of applications. The algorithm requires an additional circuit controlling the effective pedestal by increasing and decreasing a single bin depending on the comparison of the ADC value and its current pedestal. The length of the introduced counter corresponds to the compensation response time. In order to compensate mainly for the long-term drift and remain insensitive for very short time intervals, a 34-bit counter has been chosen. For a 10-bit ADC input, the fractional part then is 24 bits. The 8-bit fractional part considered in [3] seemed to be too short. For 40 MHz sampling frequency and continuous counting, the 24-bit counter will be overloaded after an interval $\tau \approx 0.4$ s. This means, in case of a permanent drift the pedestal will be compensated at a speed of ~ 2 ADC-channels/s which is sufficiently slow to not introduce short-term distortions related to real physics events with time durations of several microseconds.

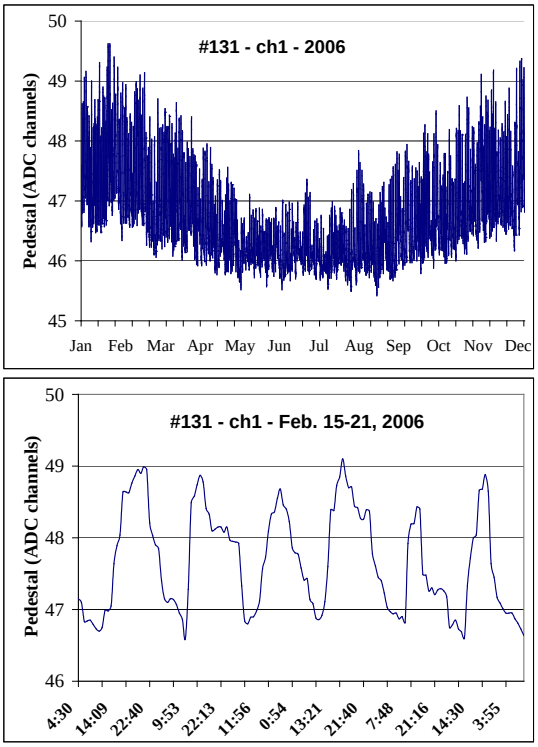

Figure 2: Dynode pedestal as a function of time (channel 1 in the Luz tank (No. 131) from Jan 1^{st} until Dec. 31^{th}, 2006) (top). Seasonal drift is clearly seen. Short-term variation of the pedestals for high-gain channel 1 in the Luz tank within Feb. 15^{th}-21^{th}, 2006 (bottom). This type of variation vs. temperature is typical for almost all Front-End-Boards in the surface detectors.

Implementation

Data from the FADCs have a 10-bit structure. In order to increase the accuracy of the final trigger, a fractional part of the compensated FADC has been taken into account as well. The performance of the full 34-bit bus (10 bits from the FADC with 24-bit fractional part) would be complicated and spendthrift. As a compromise, the output from the digital filter has been truncated to 18 bits, which will increase significantly and sufficiently the accuracy of the final trigger. The output value from the digital filter then corresponds to the compensated 10-bit integer and an additional 8-bit fractional ADC value. The 16 least significant bits are

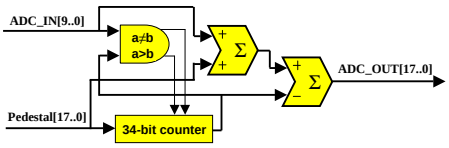

Figure 3: The digital Sigma-Delta filter. D-flip-flops corresponding to pipeline structure are not shown. The implementation is optimized to reach a sufficient registered performance, a low resources utilization as well as to minimize quantization effects due to integer inputs samples.

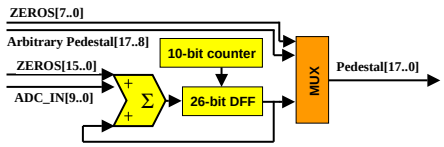

Figure 4: Pedestal selection. A native pedestal for each channel in each Front End Boards is calculated on the basis of 2^{26} samples separated by intervals 2^{10} time bins = 25.6 μs. The multiplexer allows selecting a "manual" mode with a pedestal arbitralily chosen or an "automatic" mode with pedestals optimized for each channel.

ignored (they are only used in the internal compensation circuit).

Figure 3 shows the principle mechanism of the Sigma-Delta filter. Pedestal[17..0] is a pedestal input value required for the long-term operation. Let us notice, that this variable has a real value (10-bit with 8-bit fractional part). It can be set arbitrarily to a constant value for all Front End Boards (FEB) and channels. However, the distribution of pedestal values in various FEB and channels is relatively wide. Lowest pedestals reach less than 20, highest even more than 70 ADC channels. If the pedestals in all channels would have been chosen e.g. to ADC channel 50, in some channels the measurement range would have been artificially shifted towards higher ADC values (i.e. to ADC channel 50 - 20 = 30). It means, real signals with an amplitude in the range 999...1023 ADC channels, normally not saturated, would be artificially saturated due to the applied pedestal compensation.

A simple solution avoiding above the difficulties is a pre-calcuation of the pedestal, giving the value calculated from actual data of the individual channel. The ADC data are sampled in 25.6 μs (each 1024^{th} time bin controlled by the 10-bit counter, cf. Figure 4) and summed in an accumulator. 2^{16} samples result in 26-bit data which, truncated to the 18-bit bus, can be used as the starting pedestal value (selected in MUX - see Figure 4).

The algorithm sketched above has been implemented into the AHDL code of the 3^{rd} generation Front End Boards of the Pierre Auger surface de-

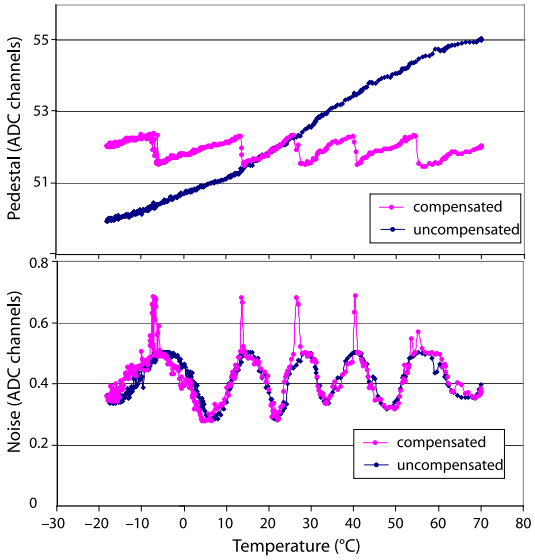

Figure 5: FADC drifts a function of temperature measured in the climate chamber. Top: The uncompensated drift range amounts to ≈5 ADC-channels. The compensated one by the sigma-delta routine stays below 1 ADC-channel. Each point in the graphs correspond to averaged pedestals over 10^5 measurements.
Bottom: Comparison of noise levels for both approaches. The peaks correspond to the narrow transition ranges, when the compensated pedestal changes due to filtering around the neighboring integer number relating to ADC input. 10^5 measurements is a overestimation and corresponds to much longer interval than is used in a real noise calculations only in order to show a tendency of a noise level. Because of a short transition range the probability, that a shower is registered exactly in a moment, when the noise increases temporarily, is negligible.

tector. The boards are equipped with Cyclone™ Altera® chips [3] and were tested in a climate chamber in the laboratory in Wuppertal. The results are satisfactory: The pedestal drift by the standard uncompensated code reaches more than 5 ADC channels. With the Sigma-Delta compensation the variation range decreases to ~ 0.8 ADC channels (see Figure 5).

The sawtooth profile observed in the compensated pedestal of Figure 5 is a consequence of the integer values obtained from the FADC. In case the FADC values fluctuate around an integer value n, one obtains on the output the required pedestal value. However, if the average pedestal increases and the FADC fluctuates around the value $n + 1$, the Sigma-Delta routine still tries to maintain the required pedestal value. Only after 2^{34} time bins with FADC values above n, the 34-bit counter changes the compensation range from $n + 1$ again to n. This quantisation effect remains. Nevertheless, the transition ranges, where the jump of the noise level is observed, is relatively narrow. The propability that a shower is detected exactly for the temparature correspopnding to the transition range is low. Furthermore, the noise jump reaches only ~ 0.2 ADC-channels so that even the increased noise level does not exceed the expected noise level of 0.8 ADC-channels.

Conclusions

The Sigma-Delta algorithm significantly improves the stability of the FADC pedestal in the Front End cards of the Pierre Auger surface detectors. The noise level as a function of temperature has similar structures in both cases, except for regions in which the counter in the filter routine changes to the next stable integer value. In these regions the noise slightly increases (Figure 5) but still remains below one ADC channel and thus still meets the requirements of the readoud cards. The relatively low resource utilization allows to implement the Sigma-Delta filter also in the 2^{nd} generation of the Frond End Boards equipped with the ACEX® PLD chips [4].

Acknowledgements

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