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100 MHz sampling 1st level SD trigger for Infill Array and Auger North based on a single progressive FPGA

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Abstract content

The proposal of a new 4th generation of the Front-End with the advanced 1st level triggers for the Infill Array of the Pierre Auger Observatory and for the Auger North is described. Newest FPGA chips offer much higher capacity of logic registers and memories, as well as DSP blocks. The calibration channel, previously supported by an external dual-port RAM, has been fully implemented into FPGA chip, through a large internal memory. In turn DSP blocks allowed on implementation of much more sophisticated spectral trigger algorithms. A single chip simplified board design, newer architecture of FPGA reduced resouces utilization and power consumption. Higher sampling in the new Front- End in comparison with previous 40 MHz designs as well as free resources for new detection algotithms can be a good platform for CR radio detection technique at Auger enhancing a duty cycle for the detection of UHECR's.

If this papers is presented for a collaboration, please specify the collaboration

Summary

Reference

Proceedings of the 30th International Cosmic Ray Conference; Rogelio Caballero, Juan Carlos D'Olivo, Gustavo Medina-Tanco, Lukas Nellen, Federico A. Sánchez, José F. Valdés-Galicia (eds.); Universidad Nacional Autónoma de México, Mexico City, Mexico, 2008; Vol. 5 (HE part 2), pages 861-864

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