Simulation on the lpGBT chip and firmware design for the new FEC of the MuonID detector in ALICE3

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Alice (A Large Ion Collider Experiment)

- **CERN's ALICE (Large Ion Collider Experiment) studies collisions between protons and heavy ions at LHC energies in order to investigate quark-gluon plasma (QGP).**
- **One of the main observables used to study the QGP is the production of quarkonia (i.e. bound cc and bb states) in Pb-Pb collisions.**



Figure: ALICE COLLABORATION, 139 countries, 147 institutions, 1,927 members.

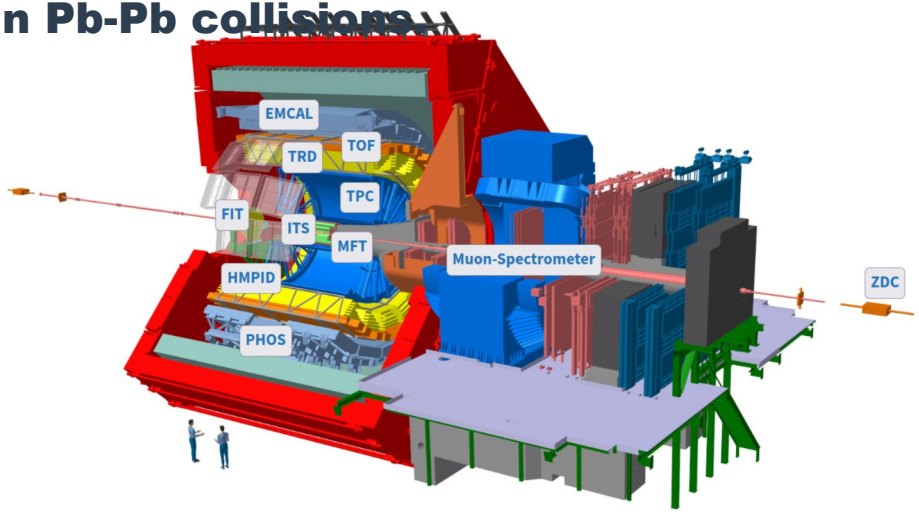


Figure: Diagram of the ALICE detectors.

ALICE3 - MuonID

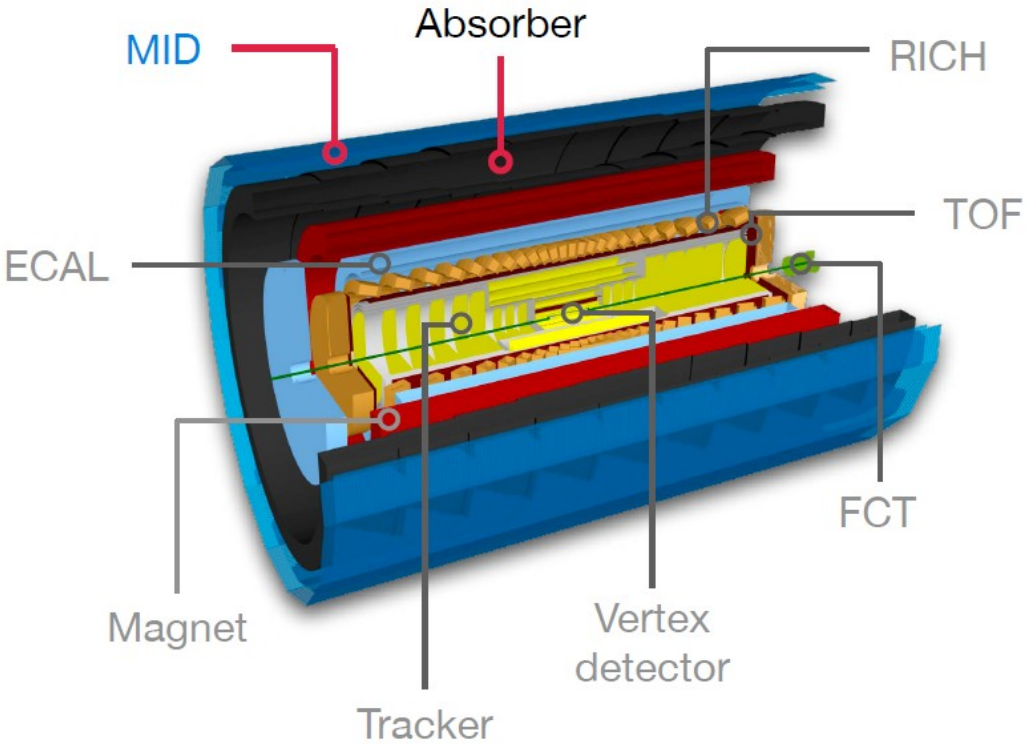


Figure: Diagram of the new detector configuration in ALICE3.

- **The main scientific focus is the study of the Quark-Gluon Plasma (QGP), including measurements of heavy-flavour production, the thermal emission of dileptons to determine the initial temperature of the collisions, and the search for phenomena such as the restoration of chiral symmetry.**

ALICE3 - MuonID

- **Reconstruction of Quarkonia**
  - **Focused on the detection of quarkonia (such as the J/ψ and Υ states) via the dimuon decay channel. This dimuon channel is superior at high transverse momenta (pT), where the identification of electrons using TOF (Time-of-Flight) and RICH (Ring Imaging Cherenkov) is limited (pT < 3 GeV/c at η = 0)**
  - **The system is optimised to identify muons down to low transverse momenta, achieving an efficiency of almost 100 per cent from pT≈1.5 GeV/c at η=0. This allows the reconstruction of J/ψ mesons with transverse momenta as low as zero.**

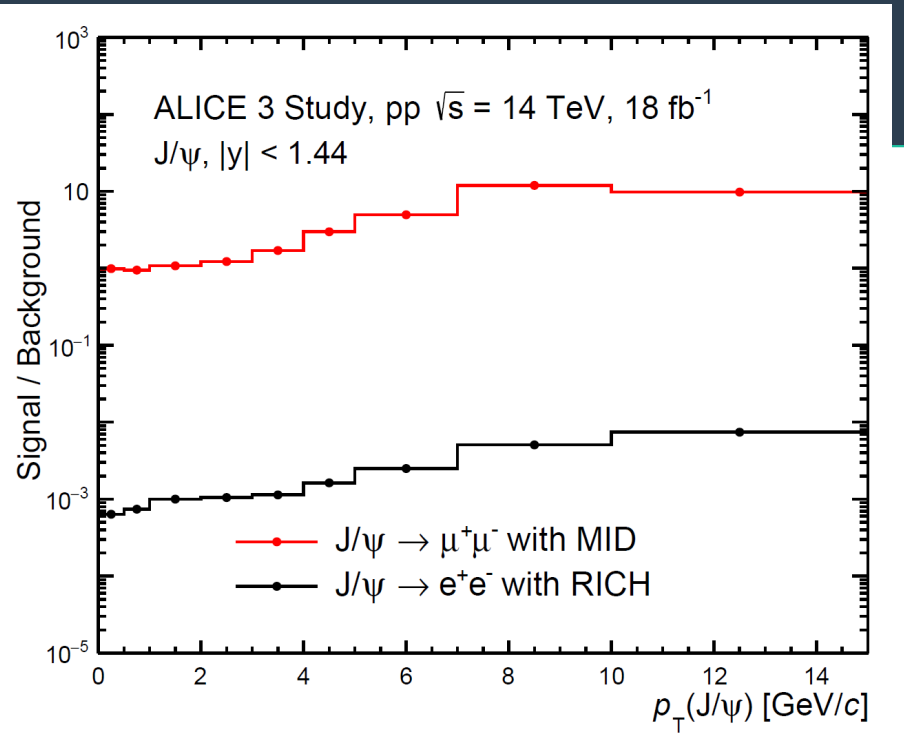


Figure: Signal-to-noise ratio of J/ψ in the dimuon and dielectron channels in pp collisions.

ALICE3 - MuonID

- **Study of Exotic Hadrons**
  - **The MID's low-momentum range allows the formation and dissociation of exotic hadrons to be investigated at thermal momentum scales; a key example is the exotic hadron χc1 (3872).**
  - **The measurement of χc1(3872) → J/ψπ+π− in the dimuon channel (using the MID) yields a signal significance that is more than ten times greater than that obtained via the dielectron channel in proton-proton collisions.**

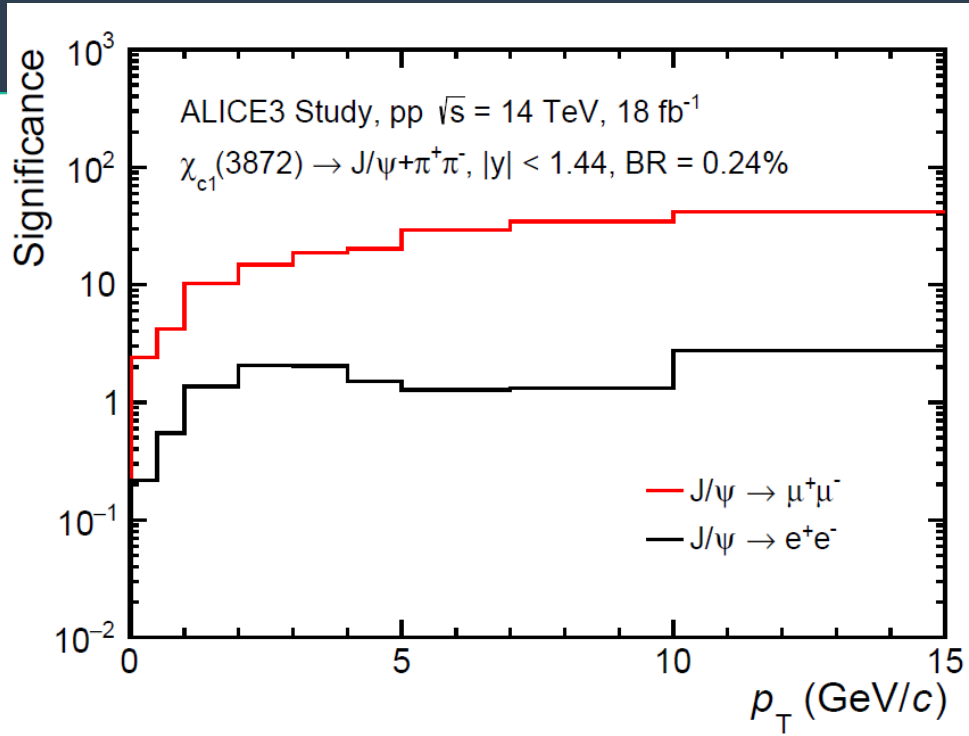
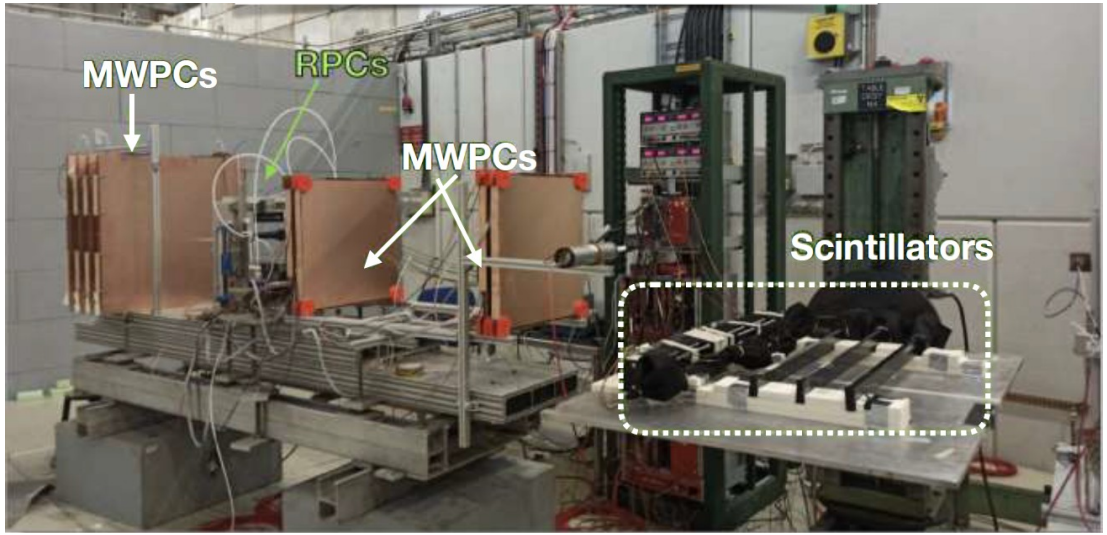


Figure: Significance for χc1(3872) → J/ψπ+π− in pp collisions (Lint = 18 fb−1).

Proposed modules



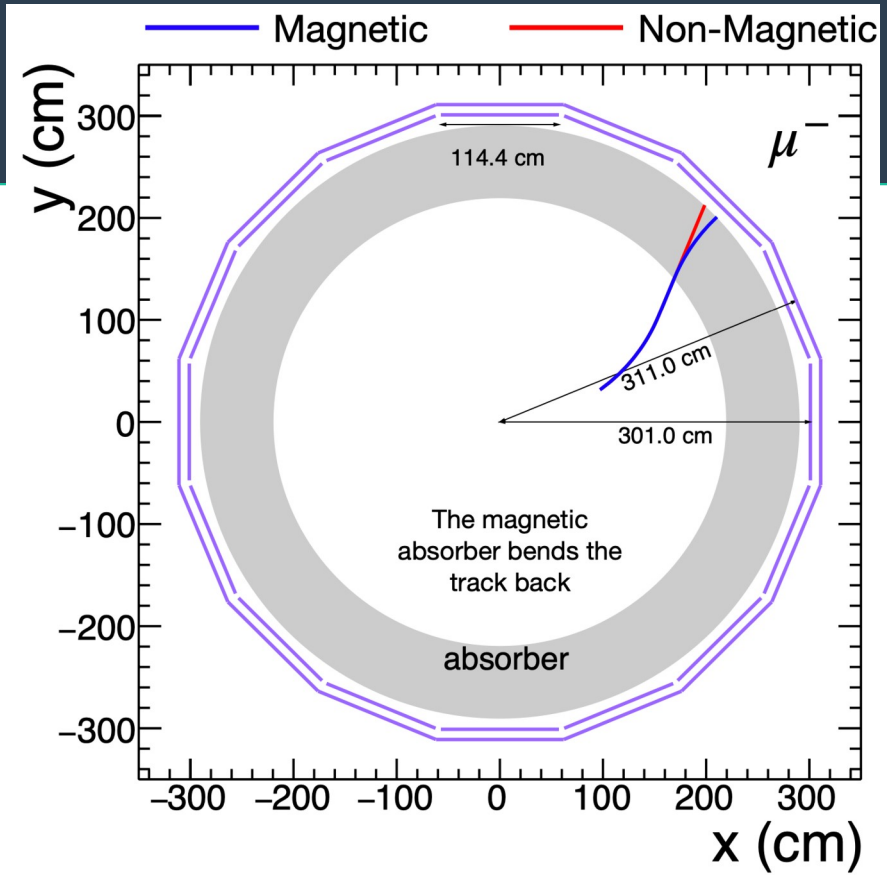


Figure: Experimental setup during the test run.

Plastic Scintillator Modules

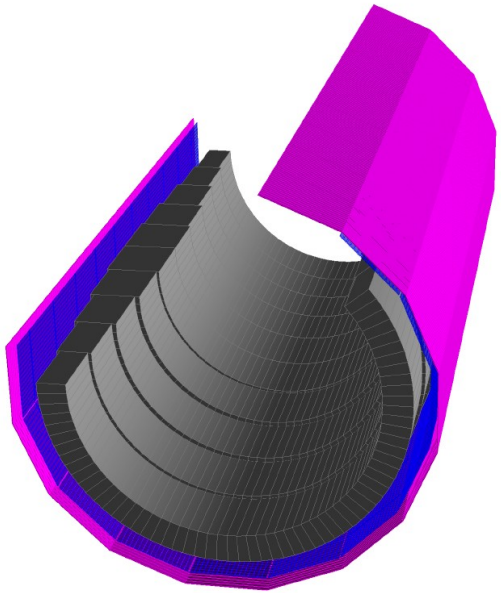


Figure: Schematic diagram of the MID detector. The 3D drawing shows the steel magnetic absorber (grey volume) and the two layers of muon chambers (shown in blue and magenta).

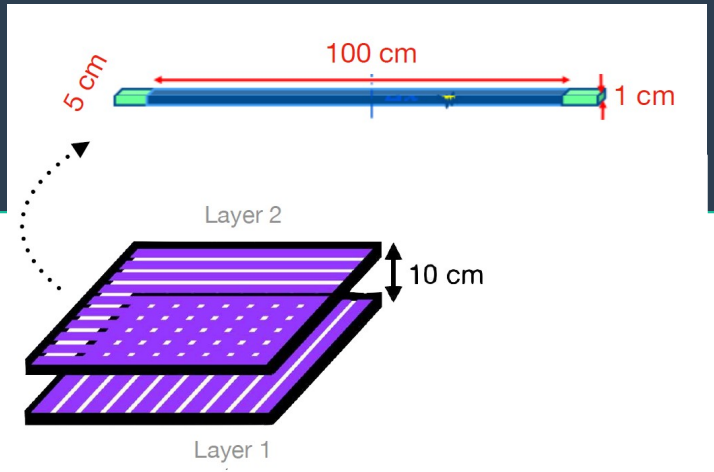
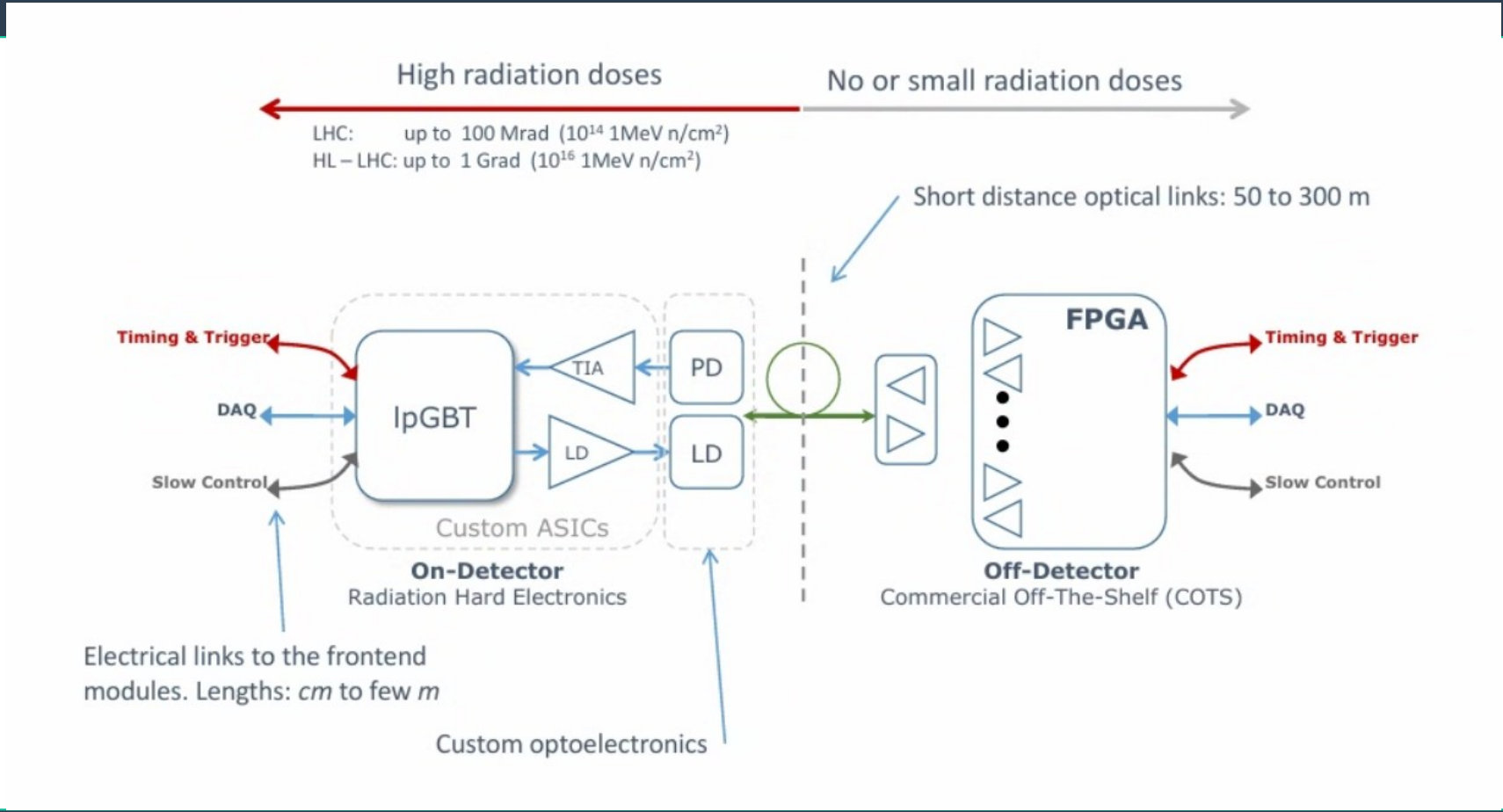


Figure: Schematic diagram of the scintillator array.

Table: MuonID Specifications

	Absorber	MID layer 1	MID layer 2
Inner radius (m)	2.20	3.01	3.11
Outer radius (m)	2.90	3.02	3.12
Total length (m)	10	10	10.5
No. of sectors in z	9	10	10
No. of sectors in φ	1	16	16
Scintillator bar length (cm)	–	99.8	123.5
Scintillator bar width (cm)	–	5.0	5.0
Scintillator bar thickness (cm)	–	1.0	1.0

LpGBT Low Power GigaBit Transceiver



LpGBT Low Power GigaBit Transceiver

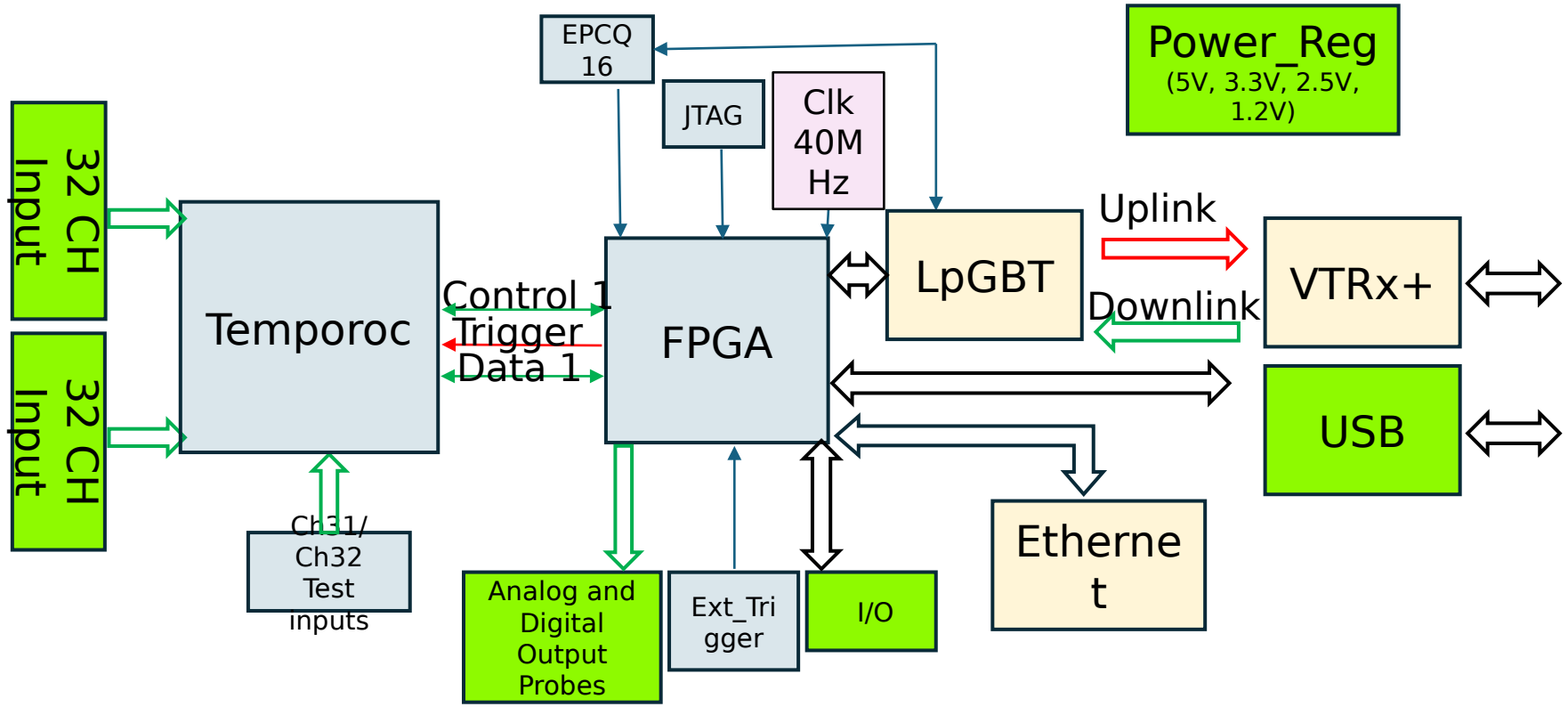
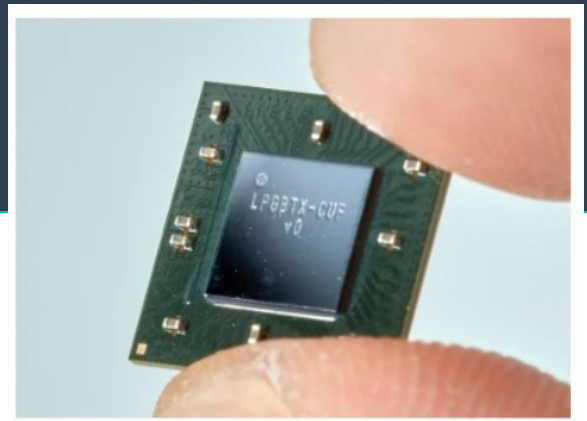


Figura .- Esquema de la FEE.

LpGBT

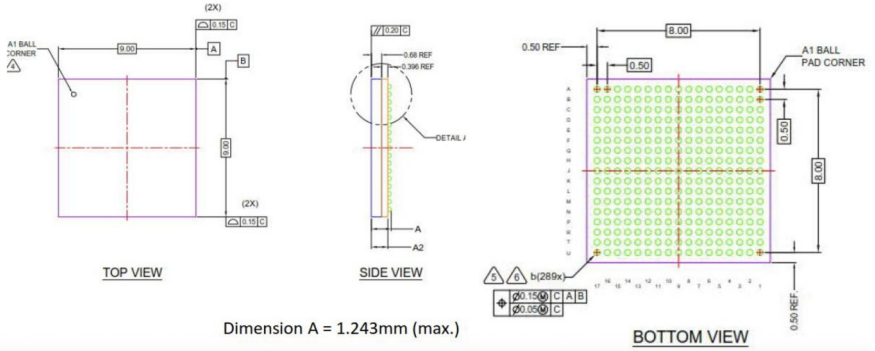


- **Capable of:**
  - 5.12 or 10.24 Gbps (for uplinks)
  - 2.56 Gbps (for downlinks)
- **Enables the implementation of RadTol links:**
  - DAQ
  - Trigger (constant and deterministic latency)
  - Experiment control [slow control]
- **Implements Control and Monitoring Functions:**
  - Three I2C Masters
  - 16 – bit General Purpose I/O port
  - Output reset pin
  - 10 – bit ADC (8 multiplexed inputs)
  - 8 – bit voltage DAC
  - 8 – bit current DAC
  - Temperature sensor

Package:

- BGA
- Fine Pitch:
  - 0.5 mm
- Pin count:
  - 289 (17 x 17)
- Size:
  - 9 mm x 9 mm x 1.243 mm

DRAFT DIMENSIONS

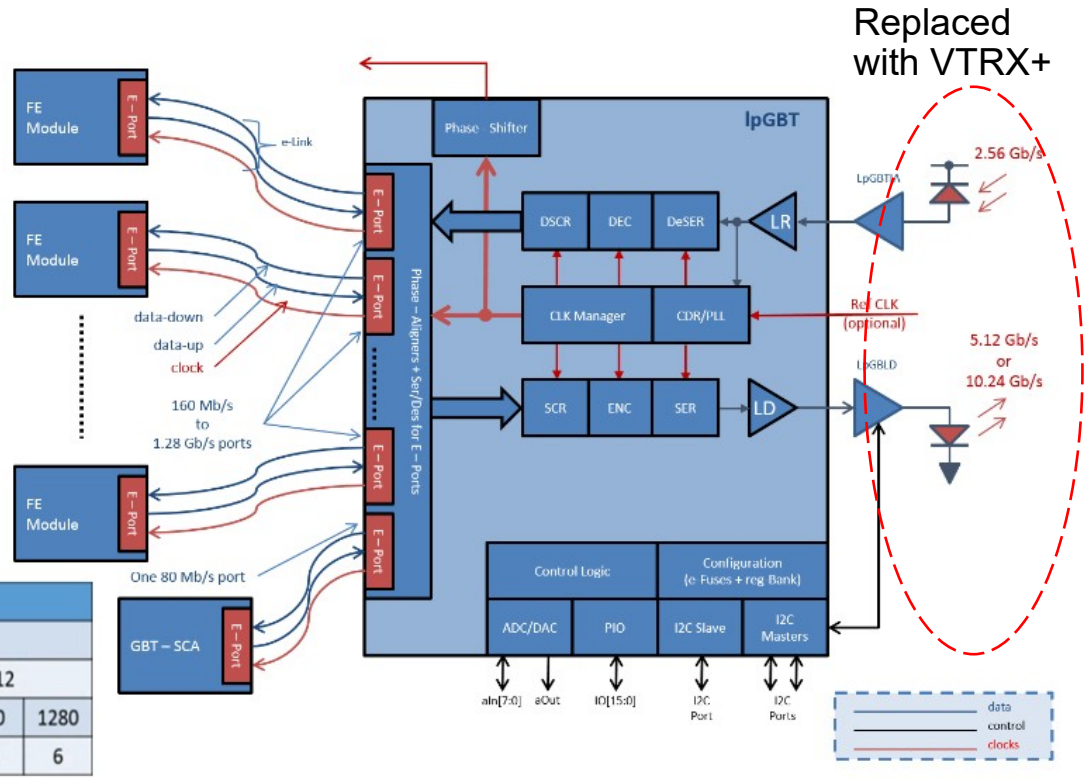


LpGBT

- **The FE modules / ASICs**
  - Electrical links (eLinks)
- **The Number and Bandwidth of**
- **eLinks is programmable**

Output eLinks (down-link)			
Bandwidth [Mb/s]	80	160	320
Maximum number	16	8	4

Input eLinks (up-link)												
Up-link bandwidth [Gb/s]	5.12						10.24					
FEC coding	FEC5			FEC12			FEC5			FEC12		
Bandwidth [Mb/s]	160	320	640	160	320	640	320	640	1280	320	640	1280
Maximum number	28	14	7	24	12	6	28	14	7	24	12	6

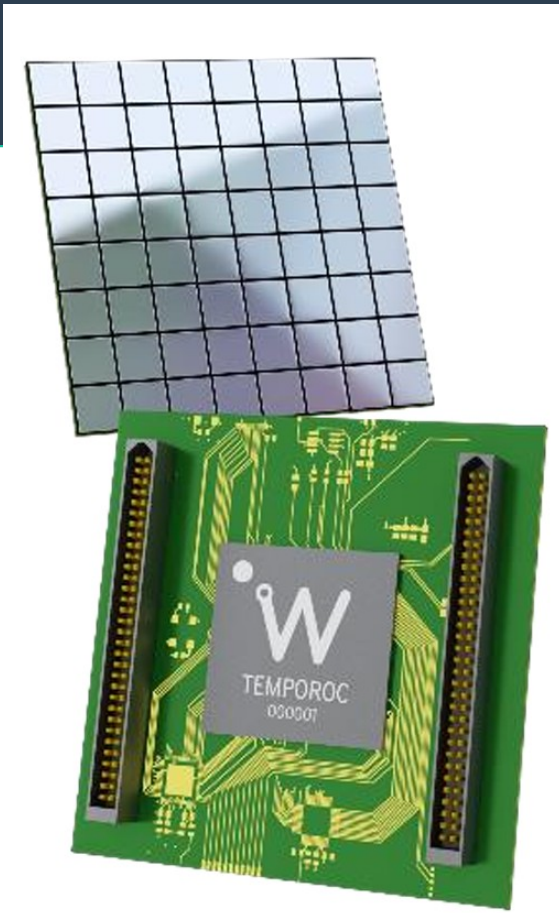


LpGBT – E Link

- **Electrical Links (eLinks) are the differential interconnections used to transmit data and clocks between the lpGBT chip and the front-end electronics**
- **They consist of differential pairs: data outputs (EDOUT), data inputs (EDIN), and clock outputs (ECLK).**
- **eLinks use the CERN Low Power Signalling (CLPS) protocol**
- **eLinks are organized into groups of four channels (eGroups)**
- **The number of eLinks and their bandwidths are asymmetric, reflecting the different upstream and downstream link capacities.**
  - There are up to 7 groups of uplink inputs (ePortRx, maximum 28 channels).
  - There are up to 4 groups of downlink outputs (ePortTx, maximum 16 channels)
- **In Transceiver Mode, the EC-port acts as a communications master to control other devices (like other lpGBTs or GBT-SCA)**
- **In Simplex Transmitter or Receiver Mode, the EC-port acts as a Listener/Talker only for ASIC configuration/control (e.g., programming internal registers)**

Temporoc

Detector Read-Out	SiPM, SiPM array
Number of Channels	64
Signal Polarity	Positive
Sensitivity	Trigger on first photo-electron
Timing Resolution	20 ps rms (TBC)
Dynamic Range	3000 photo-electrons (10^6 SIPM gain), Integral Non Linearity: 1% up to 2000 ph-e
Packaging & Dimension	Naked die – 4.9 x 11.2mm – 54.9mm^2 BGA (20x20mm, 500 balls – TBC)
Power Consumption	Power supply: 1.2V 10mW/ch
Inputs	64 voltage inputs with DC adjustment for SiPM HV tuning
Outputs	Digital output (dual ADC and dual TDC per channel) – selectable transmission mode. 1 multiplexed time trigger output 2 ASIC trigger 0R outputs (64 channels, 2 levels)
Internal Programmable Features	64 HV adjustment for SiPM (64x8bits), time trigger threshold adjustment (10bits), charge measurement tuning, ADC Peak Sensing, 64 trigger masks, internal temperature



Temporoc

Modo	Configuración (ModeRO)	Longitud Esperada
Full ADC & TDC (Default)	01111	1042 bits Incluye HADC, LADC, HTDC, LTDC, HCPT, LCPT
Hit Mode (Fast Validation)	11111	50 bits
High Gain Shaper & High Threshold TDC	01010	530 bits

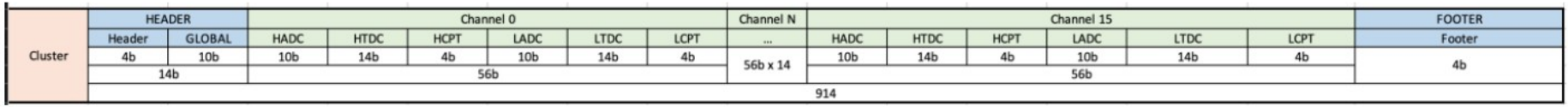


Figure 26- Full frame of digital data readout

Cluster	HEADER		HIGH LEVEL			LOW LEVEL			FOOTER
	Header	GLOBAL	Chn 0	...	Chn 15	Chn 0	...	Chn 15	Footer
	4b	10b	1b	...	1b	1b	...	1b	4b
	14b		16b			16b			
	50b								

Figure 27 - Hit data of digital data readout

Simulation on lpGBT

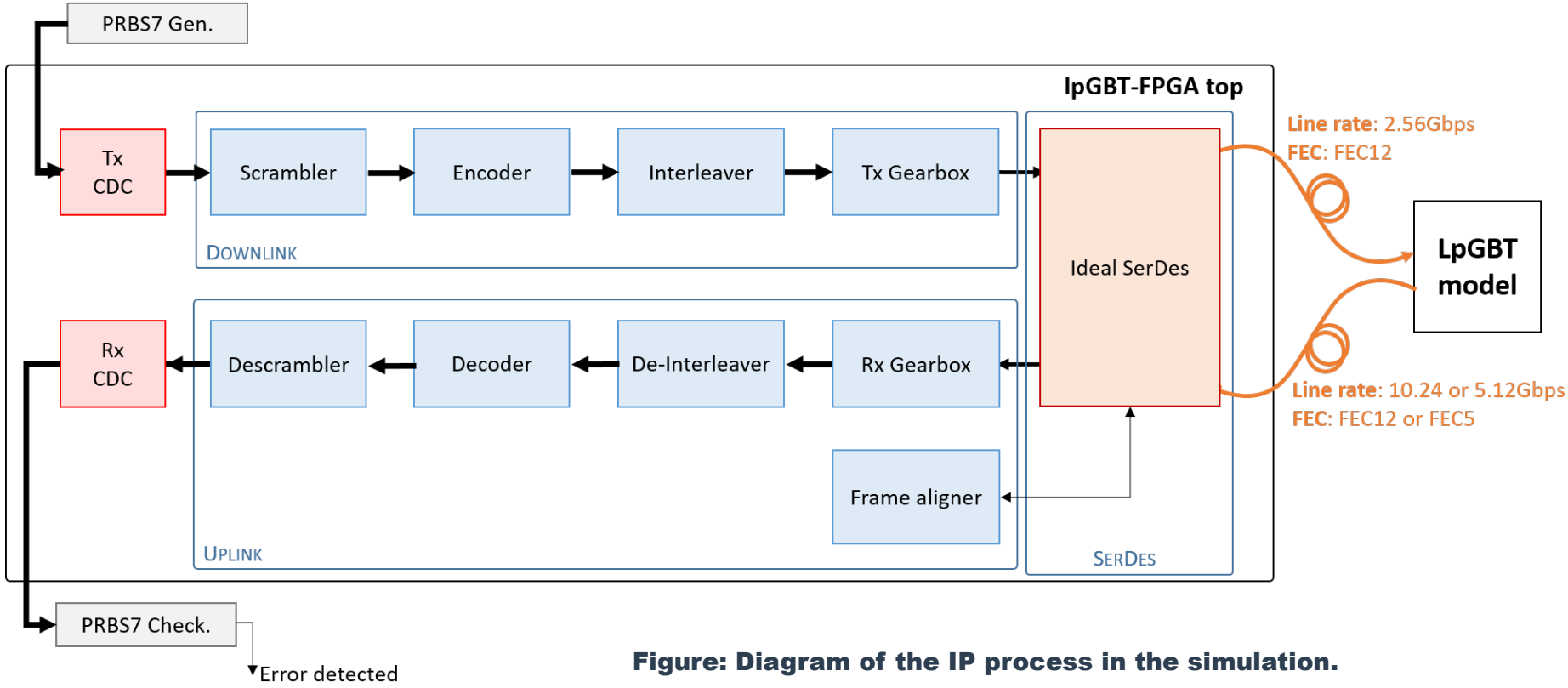


Figure: Diagram of the IP process in the simulation.

Simulation on lpGBT

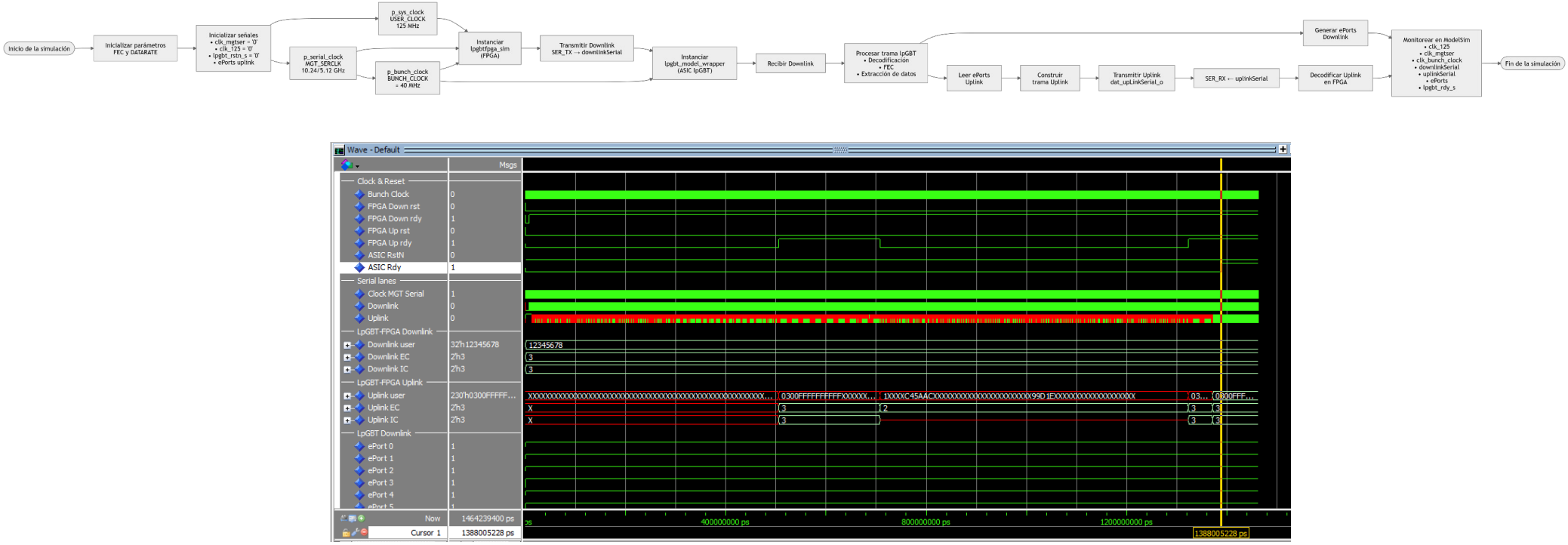


Figure: Testbench flowchart (top). View of the baseline simulation of the LpGBT IP, carried out using ModelSim software (bottom).

Uplink simulations

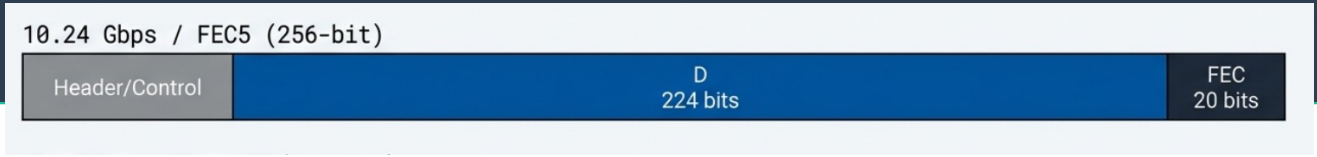


Figure: Data frame sent for use in the uplink simulation.

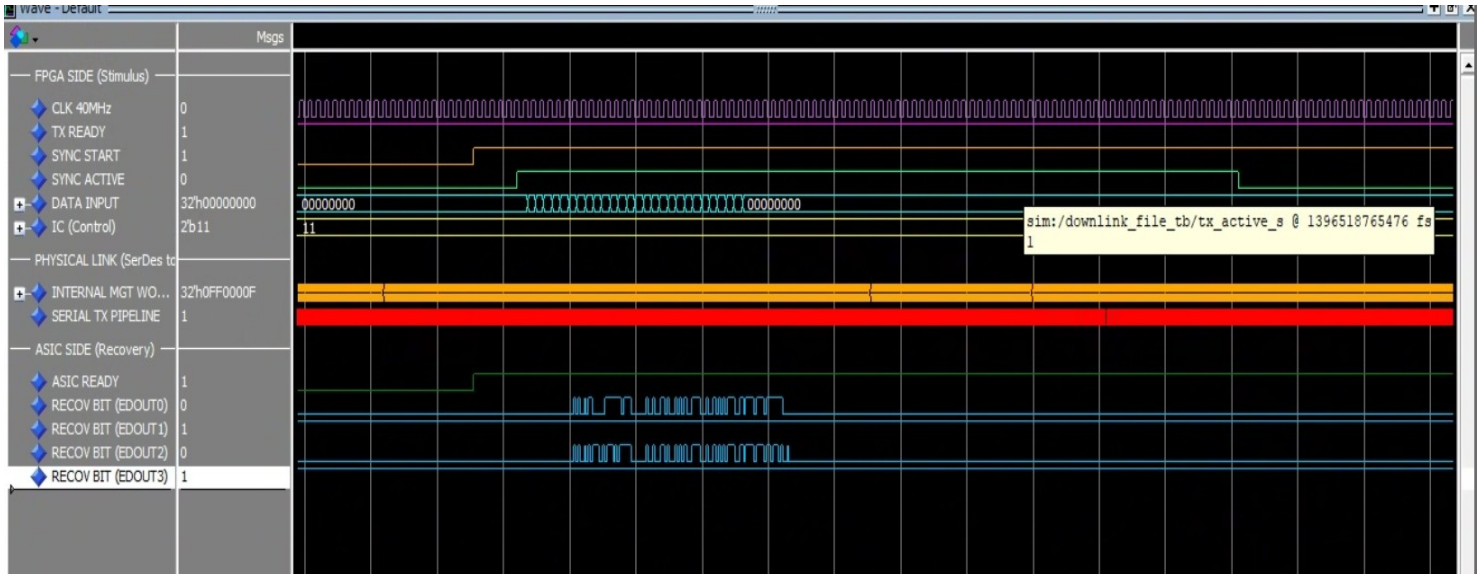
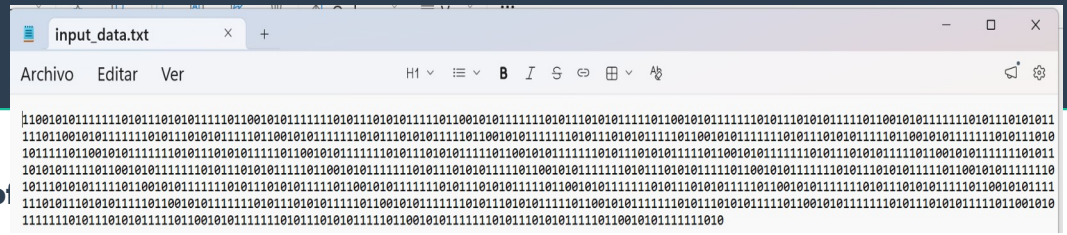
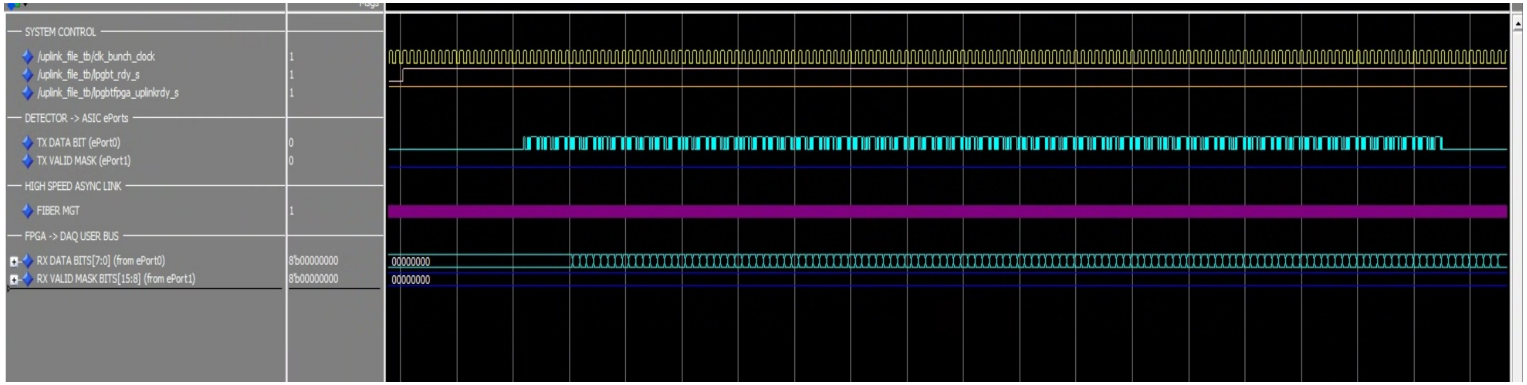


Figure: Simulation of the Slow Control transmission for LPGBT programming.

Downlink Simulation

A data frame generated by the Temporoc ASIC chip, consisting of a header, data per channel and a footer.





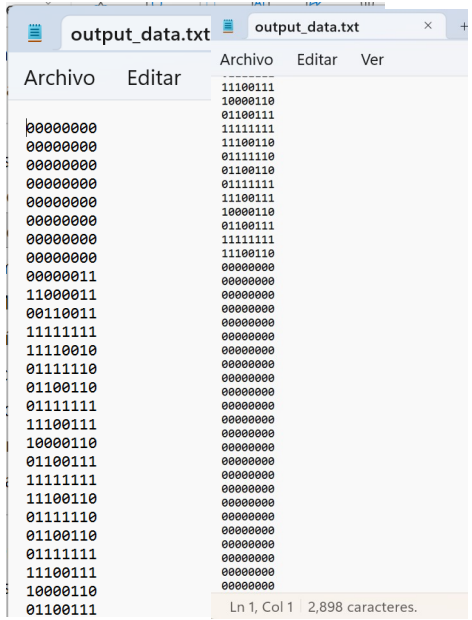


Figure: Simulation of the downlink by injecting a data file with the same structure as the data sent by the Temporoc chip.

E-links simulation module

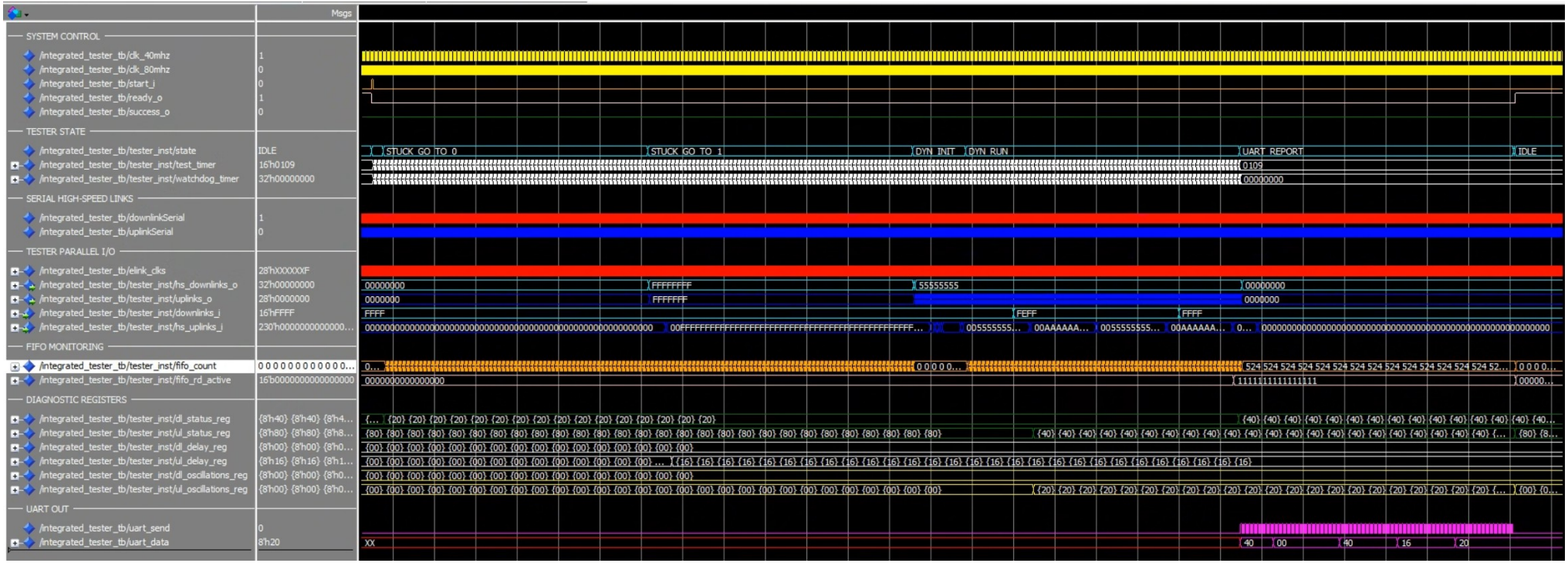
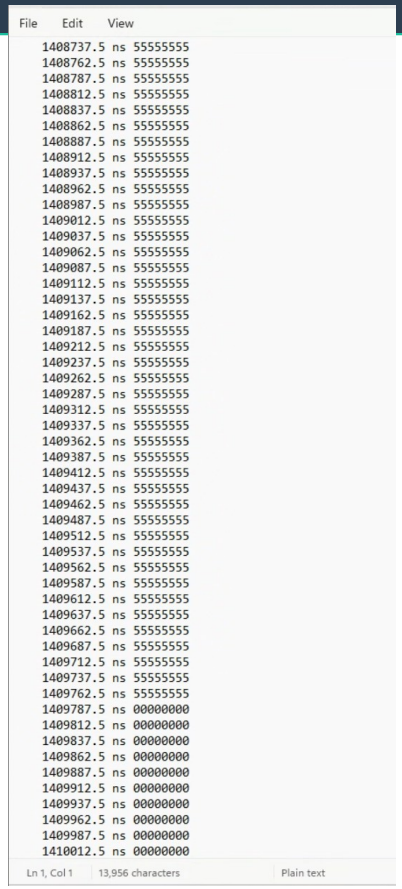
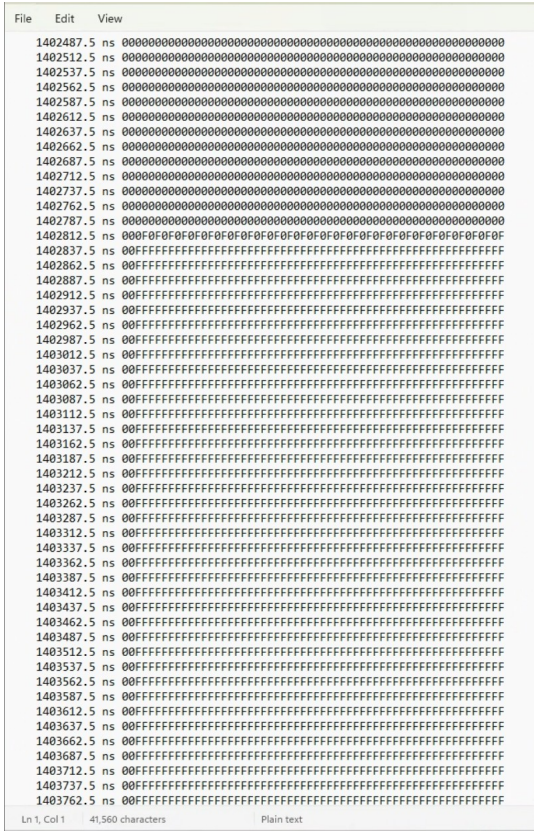


Figure: Simulation of signals for downlink and uplink testing

E-links simulation module







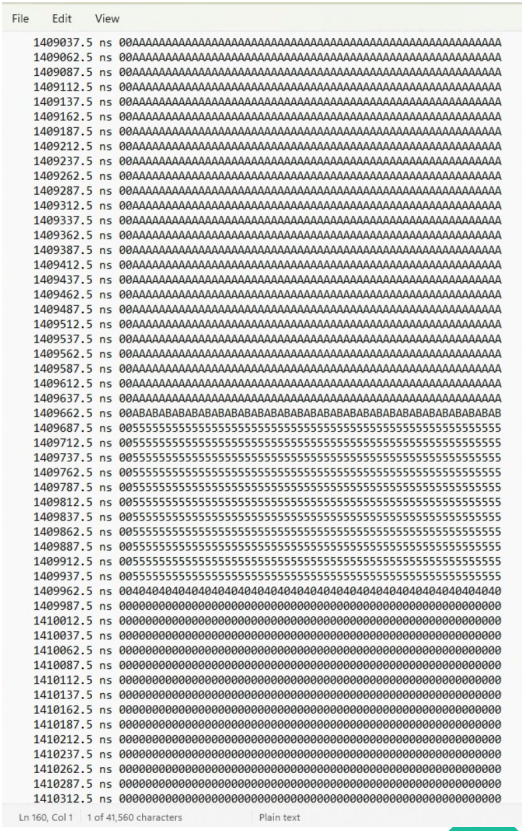


Figure: Screenshot of the downlink output file.

Figure: Screenshot of the Uplink output file.

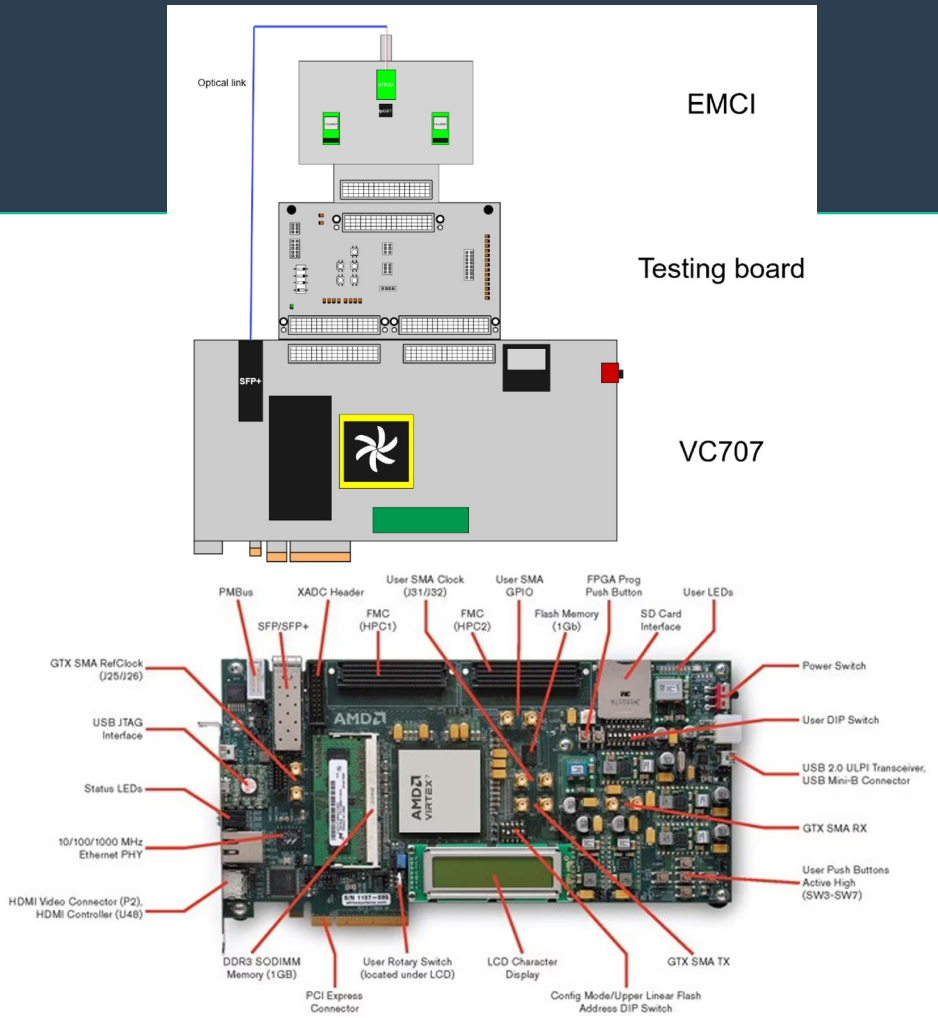


Figure: VC707 FPGA alongside the evaluation board.

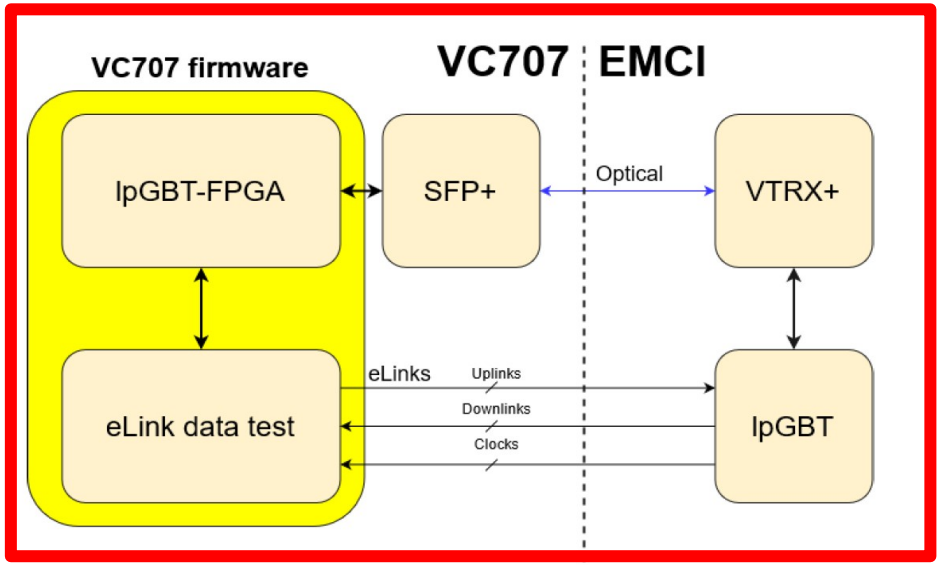
Key Features & Benefits

- 40Gb/s Connectivity platform for high-bandwidth and high-performance applications using Virtex 7 VX485T FPGAs
- Hardware, design tools, IP, and pre-verified reference designs
- Supports embedded processing with MicroBlaze, soft 32bit RISC
- Enabling serial connectivity with PCIe Gen2x8, SFP+ and SMA Pairs, UART, IIC
- Advanced memory interface with 1GB DDR3 SODIM Memory up to 800MHz / 1600Mbps
- Develop networking applications with 10-100-1000 Mbps Ethernet (GMII, RGMII and SGMII)
- Expand I/O with the FPGA Mezzanine Card (FMC) interface

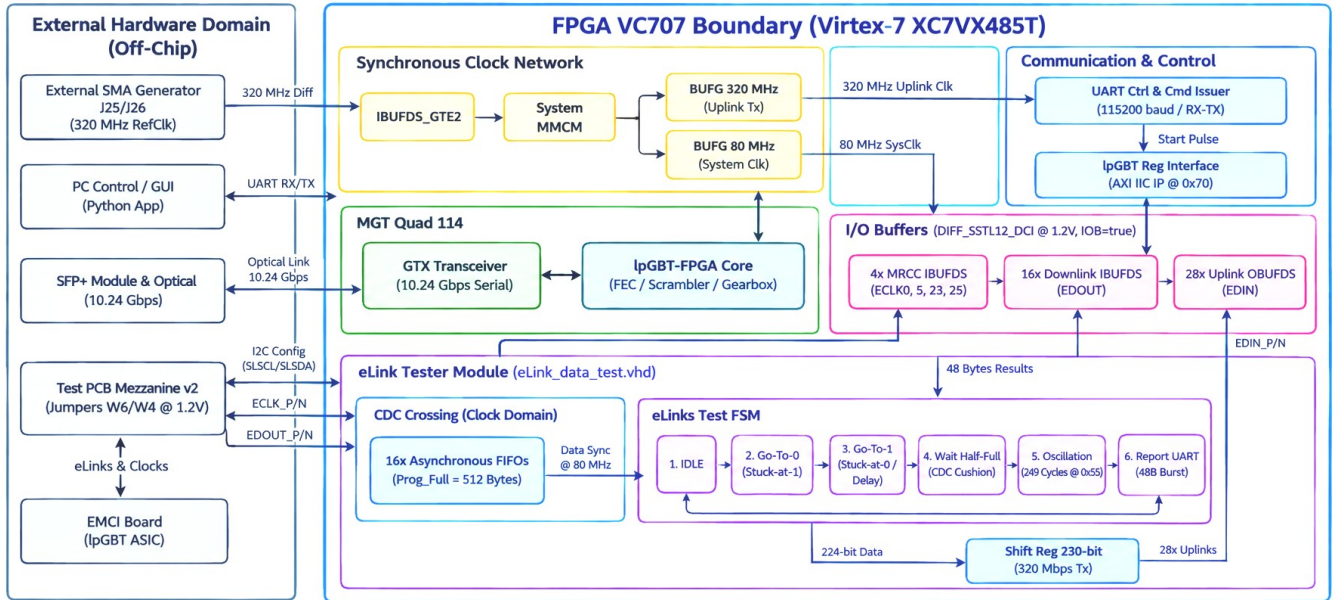
Featured AMD Devices

Featuring the ROHS compliant kit including the XC7VX485T-2FFG1761 FPGA

Logic Cells	485,760
Memory (Kb)	37,080
DSP Slices	2,800
GTX 12.5 GB/s Transceivers	56
I/0 Pins	700



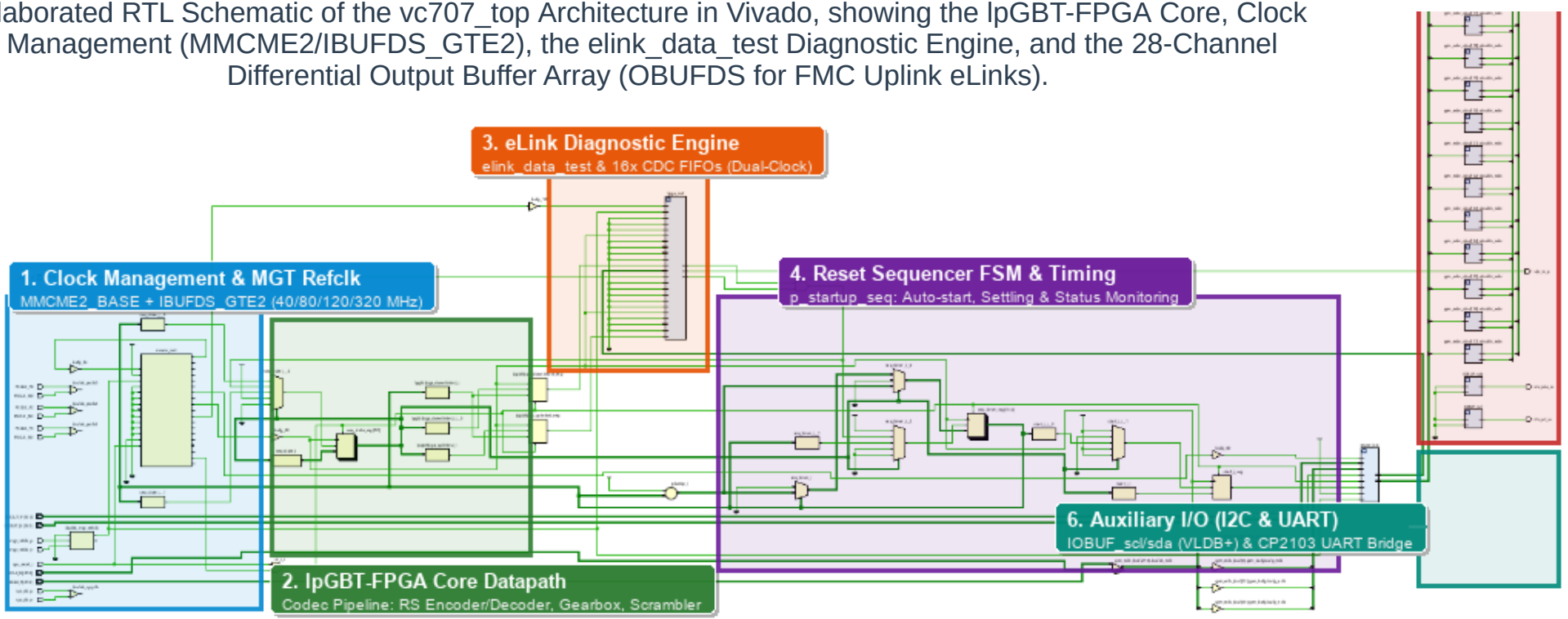
Elink Test Module



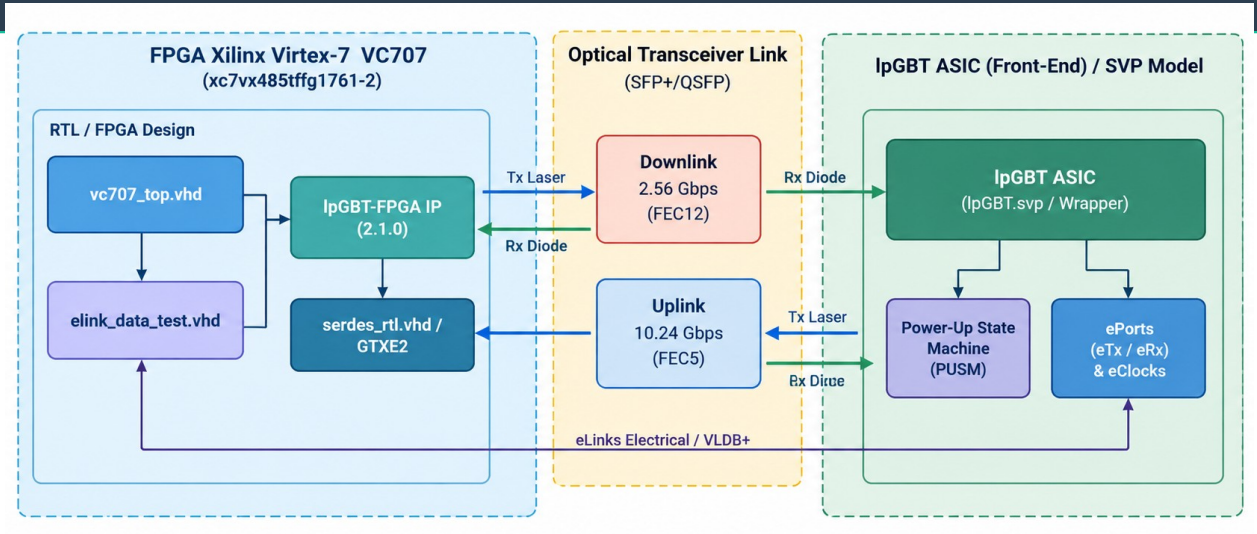
System architecture of the VC707 FPGA platform for lpGBT communication and eLink testing, including clock generation, high-speed serial communication, differential I/O, control interfaces, and the eLink test module.

RTL Schematic on VC707

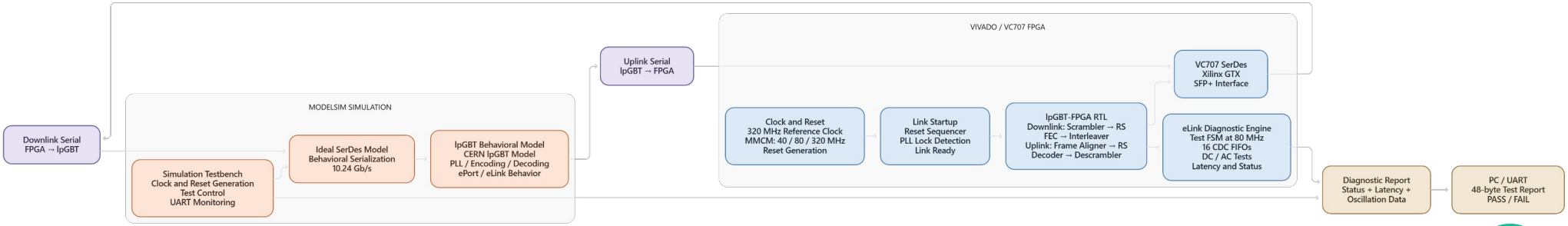
Elaborated RTL Schematic of the vc707_top Architecture in Vivado, showing the lpGBT-FPGA Core, Clock Management (MMCME2/IBUFDS_GTE2), the elink_data_test Diagnostic Engine, and the 28-Channel Differential Output Buffer Array (OBUFDS for FMC Uplink eLinks).



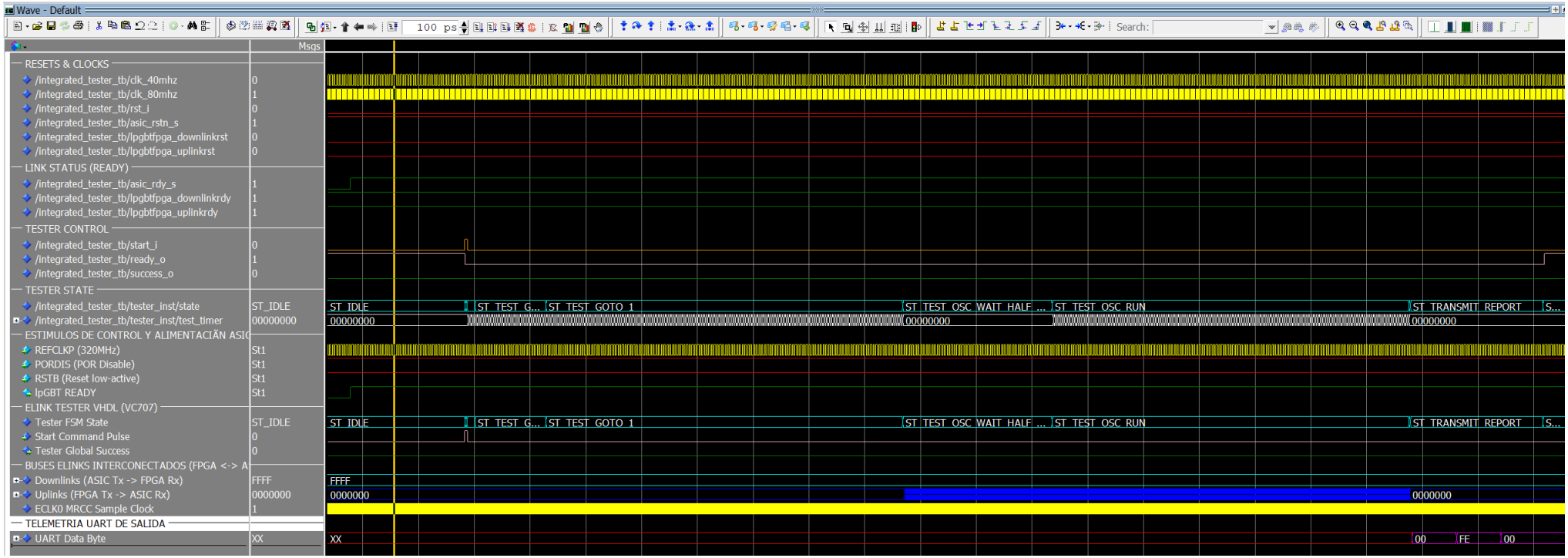
Simulation on VIVADO



FPGA–lpGBT communication and verification architecture, showing the VC707 RTL implementation and its interaction with the behavioral lpGBT model in ModelSim.



Simulations



Thank you.