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Simulation of the lpGBT chip and firmware design for the new FEC of the MuonID detector in ALICE3

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Abstract

The MuonID detector at ALICE3 at CERN, designed to identify muons beyond the 70-cm absorber and operate in triggerless mode, requires electronic systems capable of handling up to 6,400 channels with high granularity (50–60 mm/pad). In this context, simulation of the lpGBT chip is essential for validating the new Front-End Card (FEC), ensuring high-speed optical links of up to 10 Gb/s, low latency, and precise synchronization with continuous acquisition systems. The simulation focuses on studying the eLinks signals, which are configurable between 80 Mb/s and 1.28 Gb/s, evaluating their integrity, latency, and robustness against noise. Additionally, the firmware design principles for uplink (10.24 Gb/s) and downlink (2.56 Gb/s) transmission are analyzed, along with the stability of the eClocks that synchronize the input/output channels. This work enables the optimization of communication protocols and ensures compatibility with FPGA- and ASIC-based architectures—a critical step for the stable operation of the MuonID detector under high-particle-density conditions and for the efficient reconstruction of tracks in the ALICE3 experiment.

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