ALICE3 MuonID readout Electronics (plastic scintillator option)

November 25, 2024

G. Tejeda

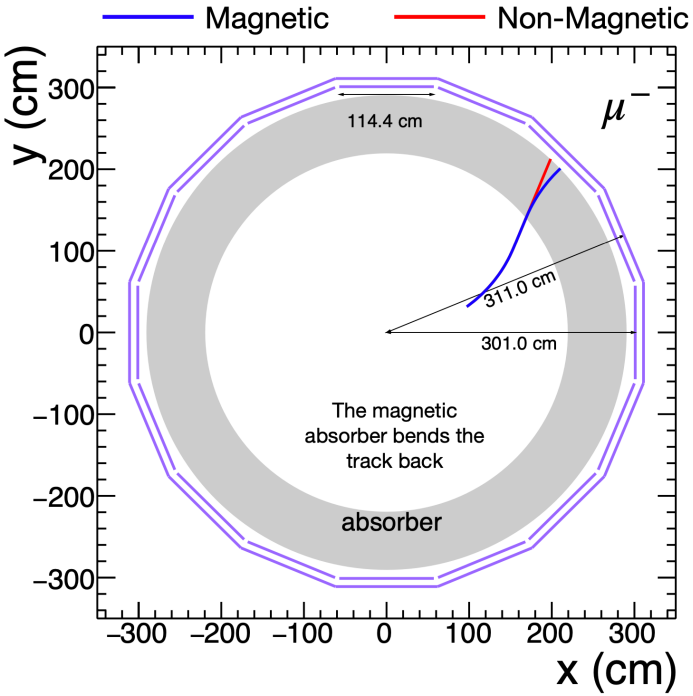
ALICE Mexico Day 2024

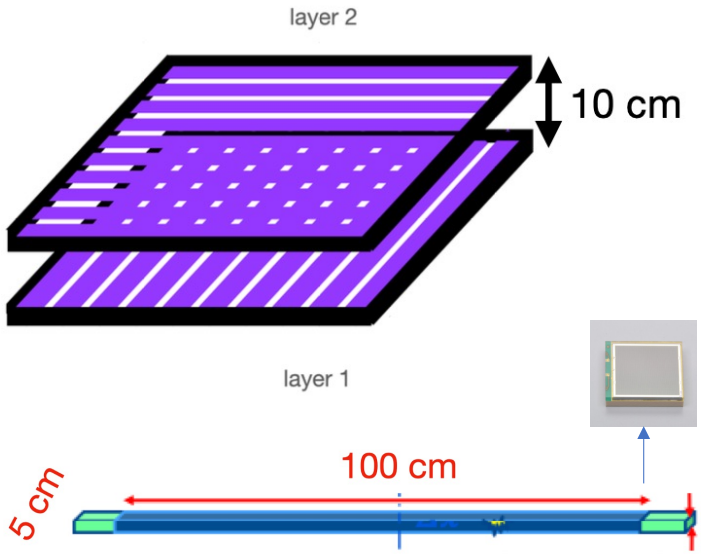
Outline

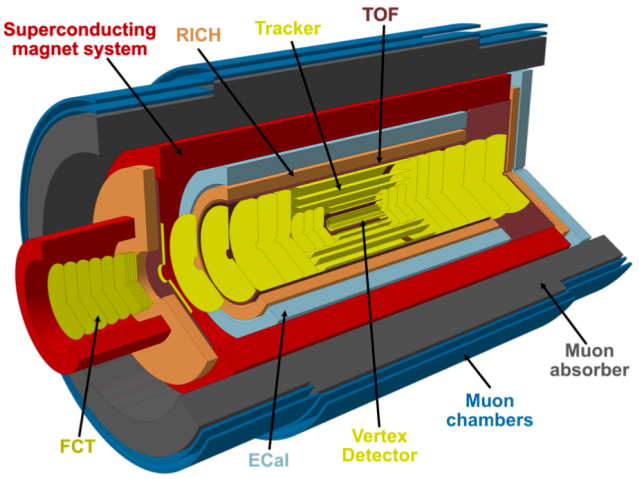
- Introduction
- MuonID Detector
- FEC specifications
- FEC Version 1
- PCB test
- Assembly status
- Parch Pannel
- User Interface
- FEC Version 2
- MuonID electronics group

MuonID Detector

Plastic Scintillator Option





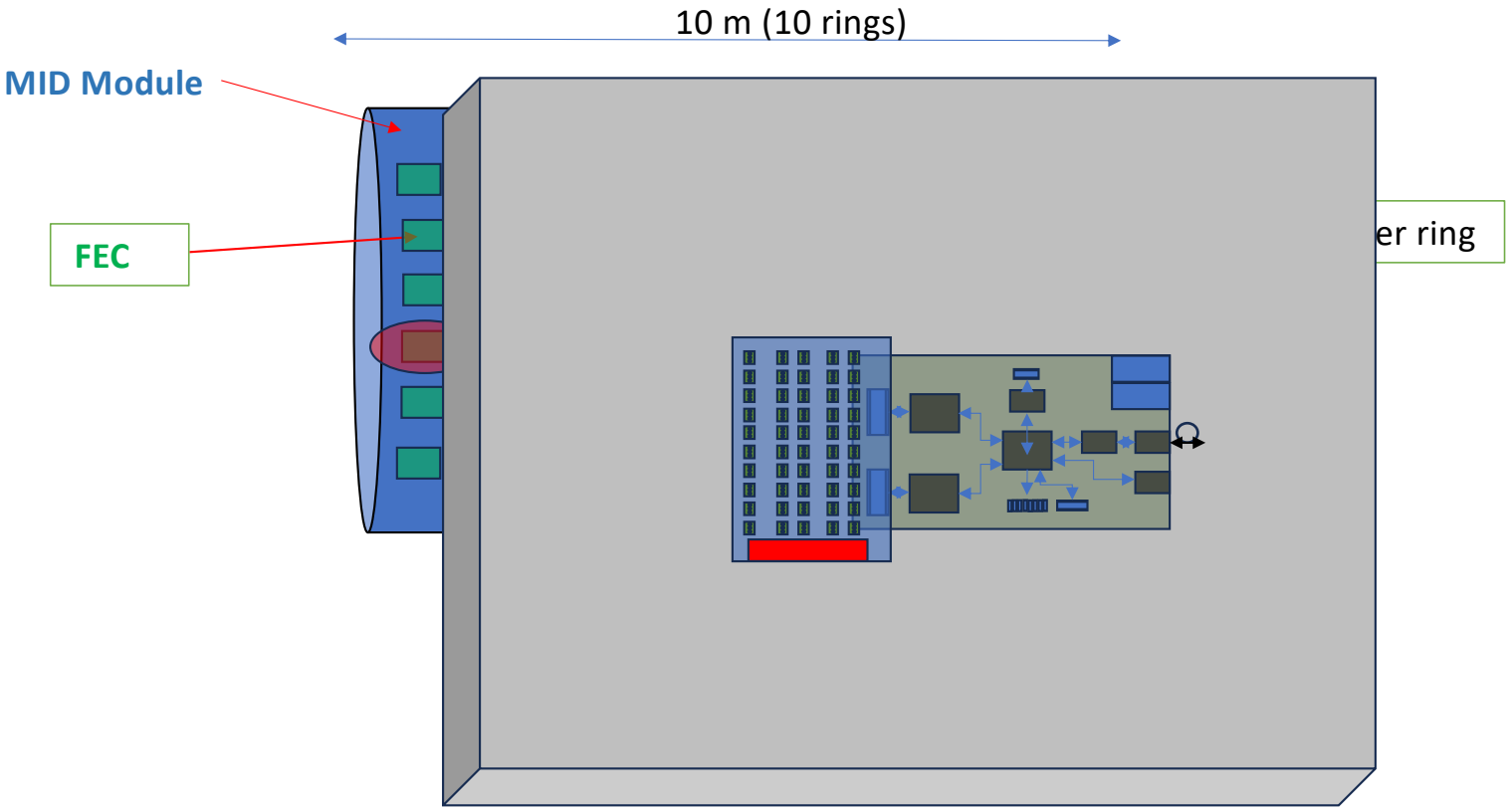


- Assumptions:
  - 10 rings
  - 16 segments per ring
    1 chamber per segment
    40 channels per chamber

FEC Specifications (V1)

- Designed for SiPM ReadOut
- 32 Channels
- 18 ps time resolution
- Signal polarity: Positive and negative
- Sensitivity: Voltage input amplifier (programable)
- Dynamic Range: 160 fC up to 400 pC
- Charge and time measurement
- Power Consumption: 6 mW/channel

Channels Distribution (Option)



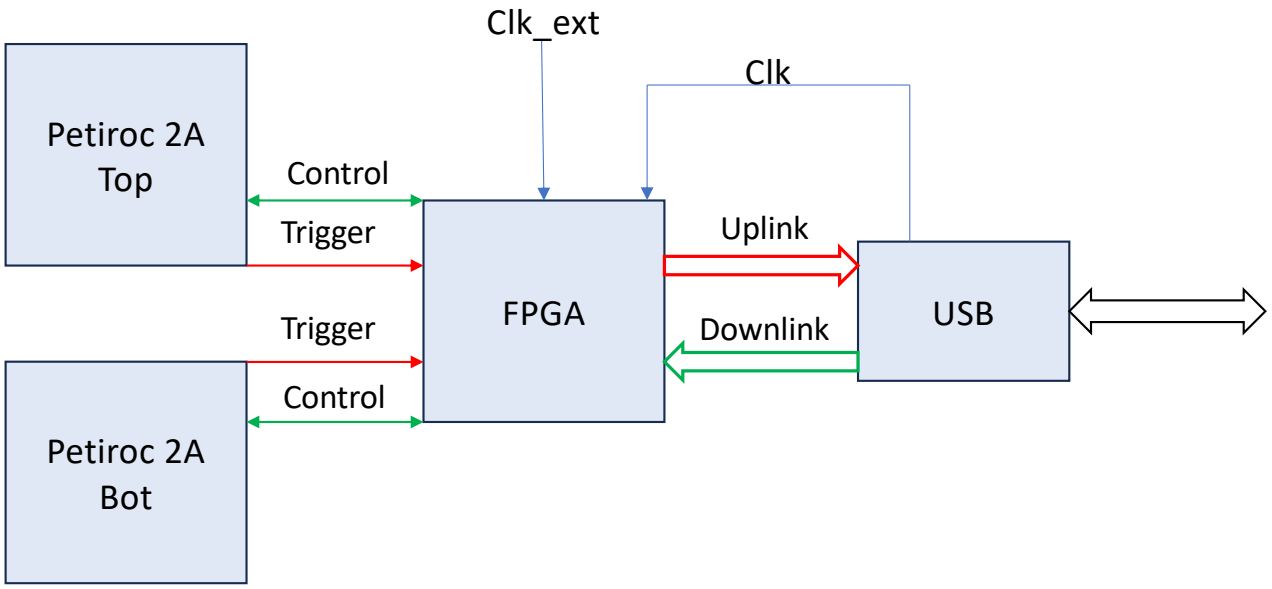
160 FECs in total

40 channels/FEC

Energy & Time measuremnt

Required 160 optical links for all modules

MuonID FEC details



1 FEC/Module 160 (10 spares) FEC in total

2 Erni connectors with 32 ch each

2 ASIC Petiroc 2A

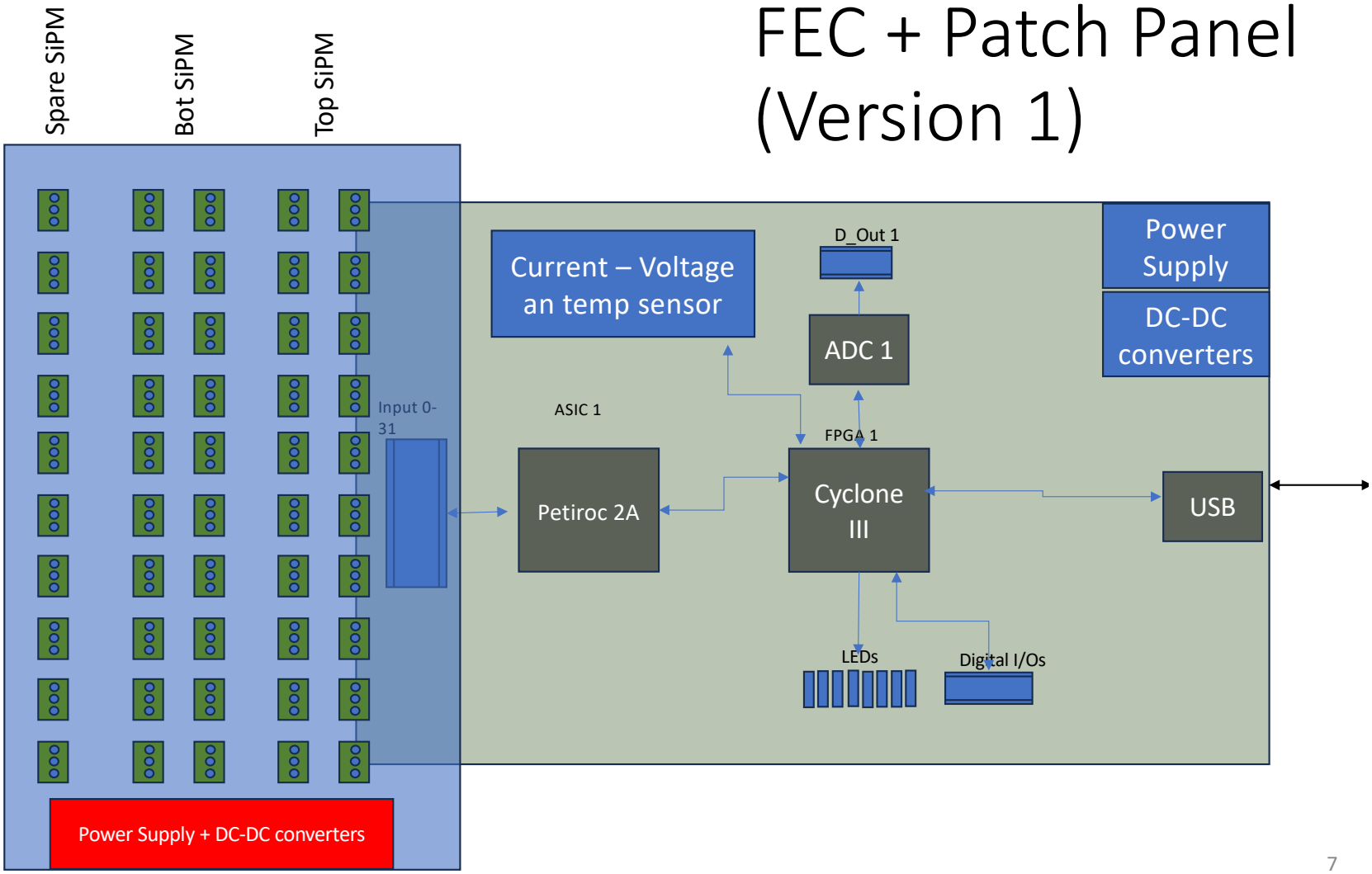
1 FPGA Cyclone V
(non Rad-Hard 5cgtfd5c5f23c7n)

1 LpGBT + VtRx
(for communication and Slow control)

Power supply regulators zone

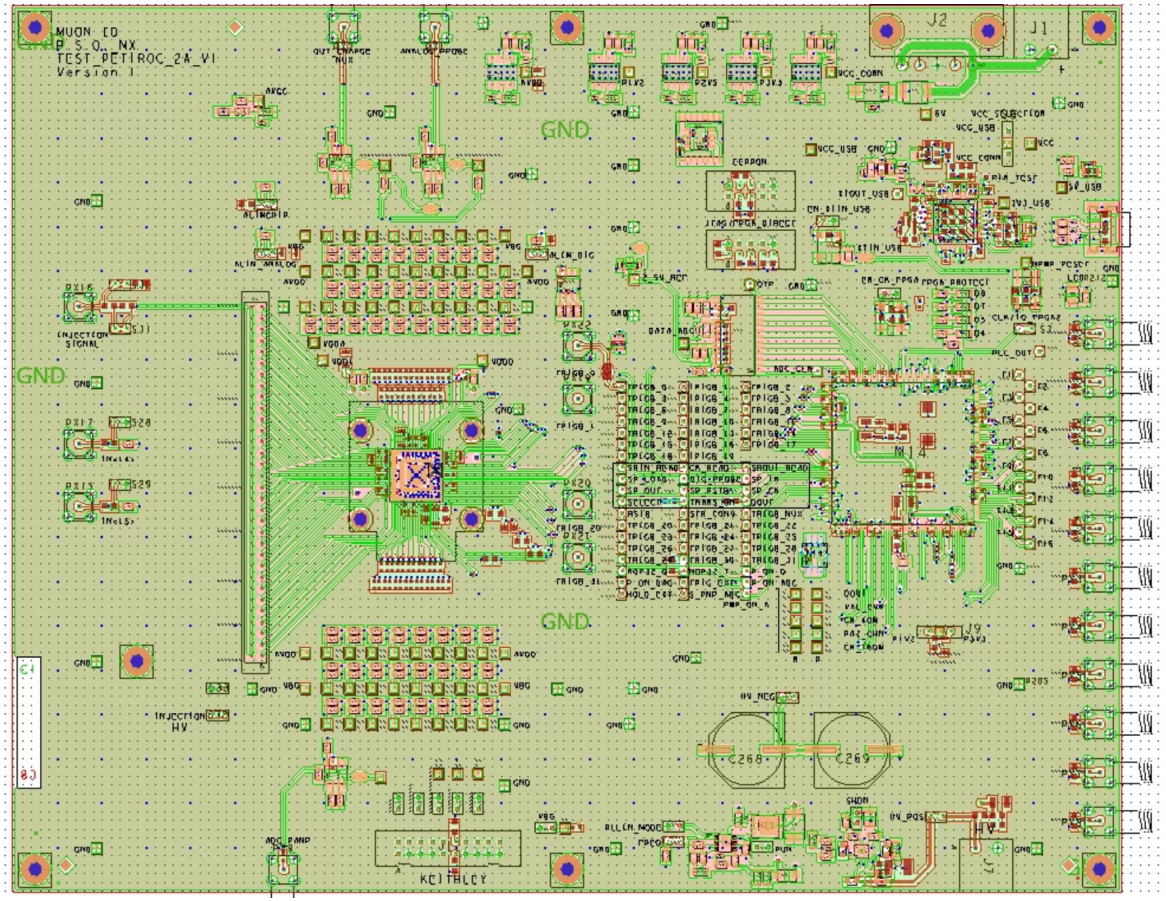
FEC + Patch Panel (Version 1)

- 1 ASIC Petiroc 2A
- 1 FPGA Cyclone III (non Rad-Hard)
- USB communication and debugging
- 32 Channels input
- Charge and Time measurements
- Channel by channel SiPM high voltage adjustment
- 6mW/channel power consumption



FEC
Final Design

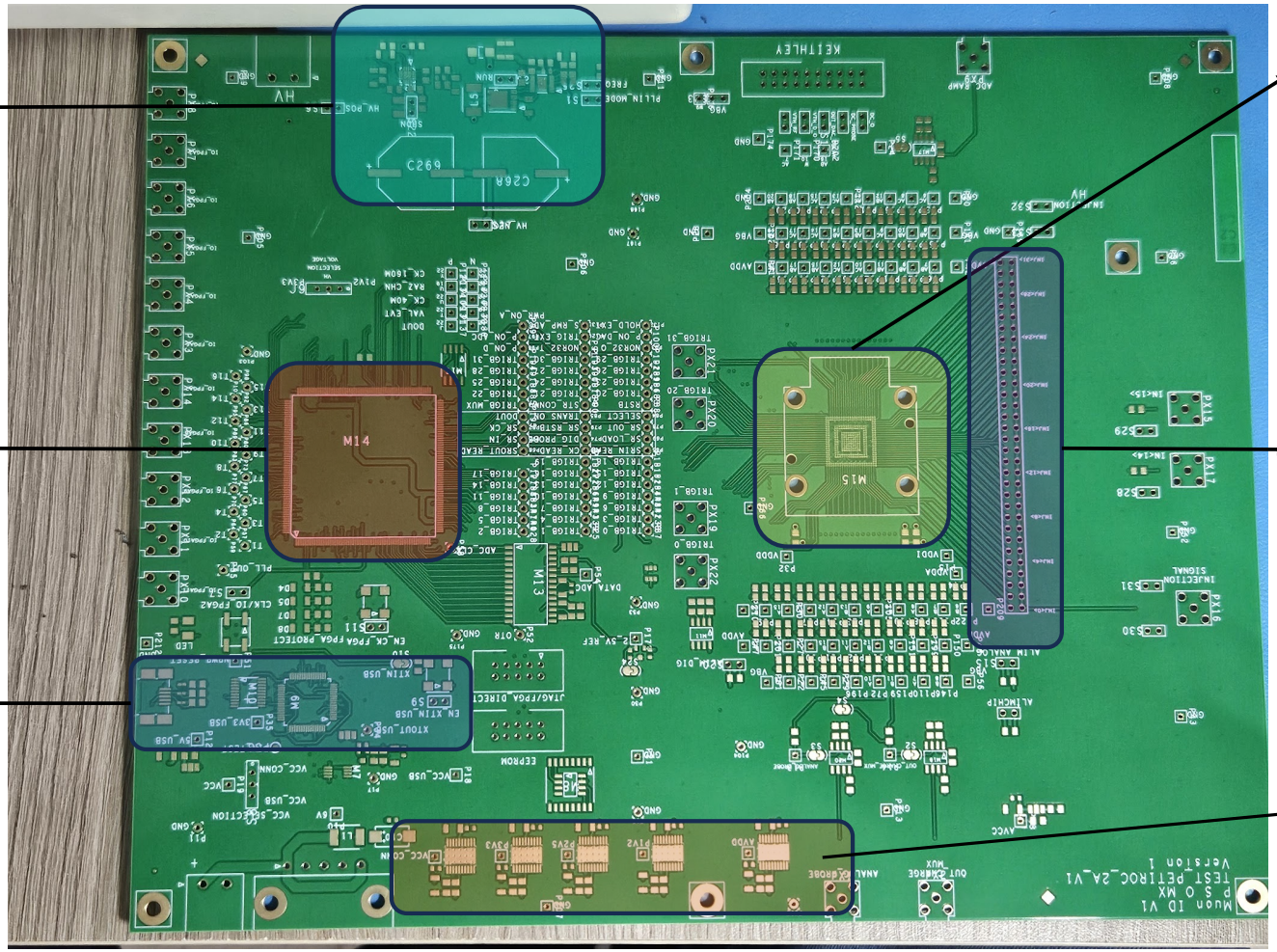
- 25 x 20 cm
- 1 PETIROC 2A (32 Ch)
- FPGA Cyclone



HV regulators

FPGA

USB port

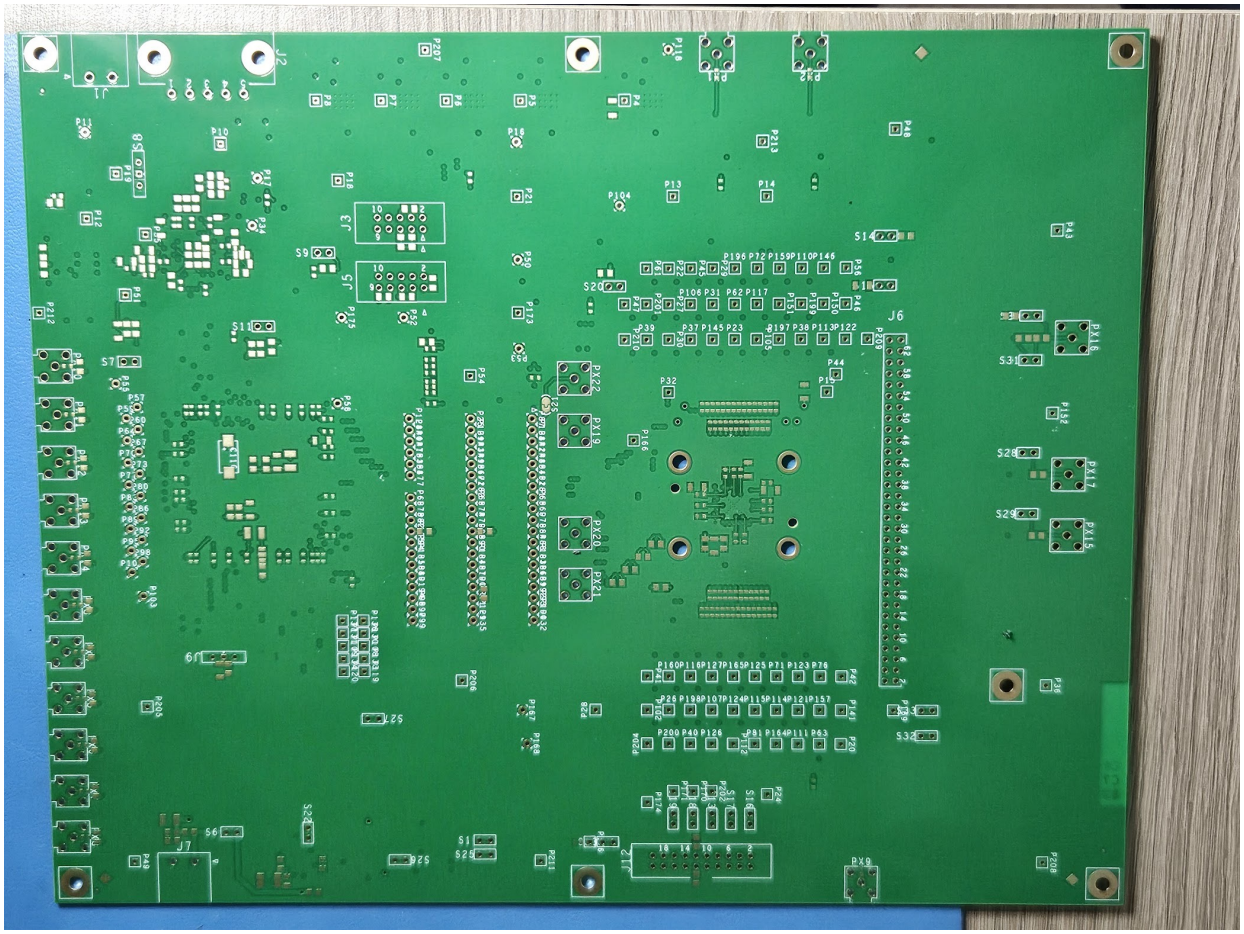


Petiorc 2A

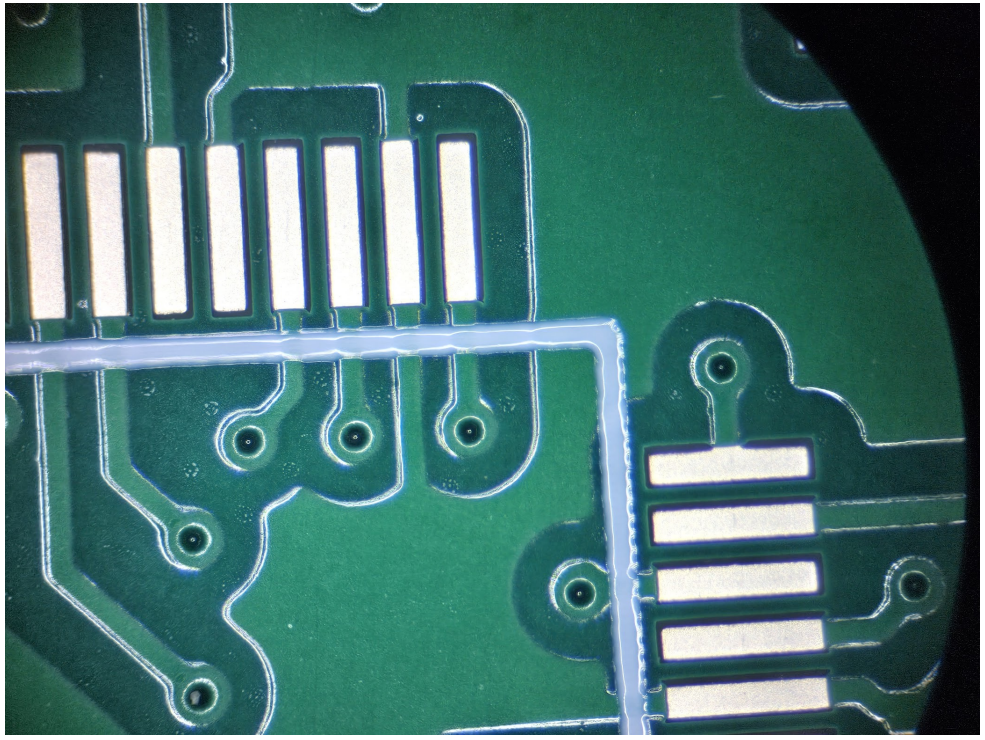
32 inputs connector

Low Voltage Power regulartor (1.2V, 2.5V, 3.3V and 5V)

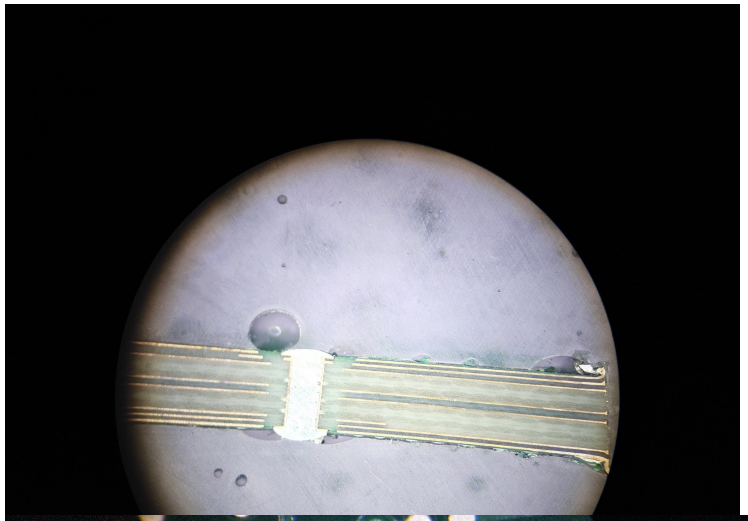
Bottom View



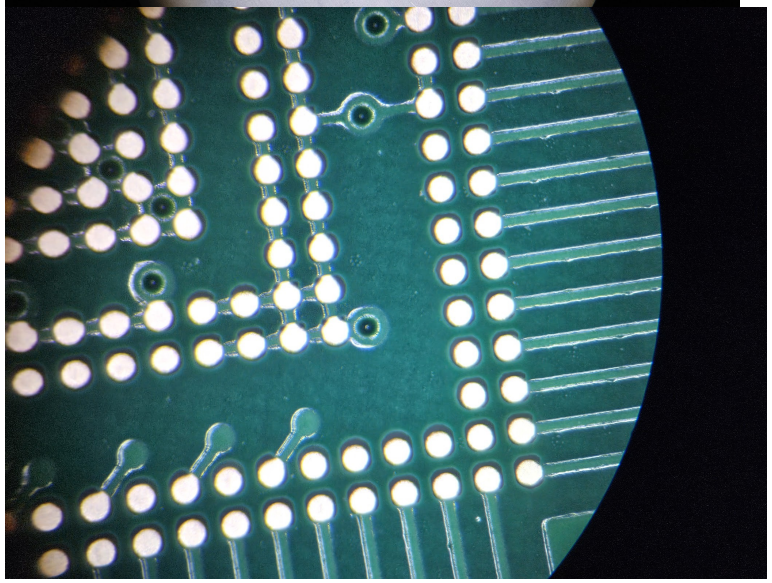
PCB test



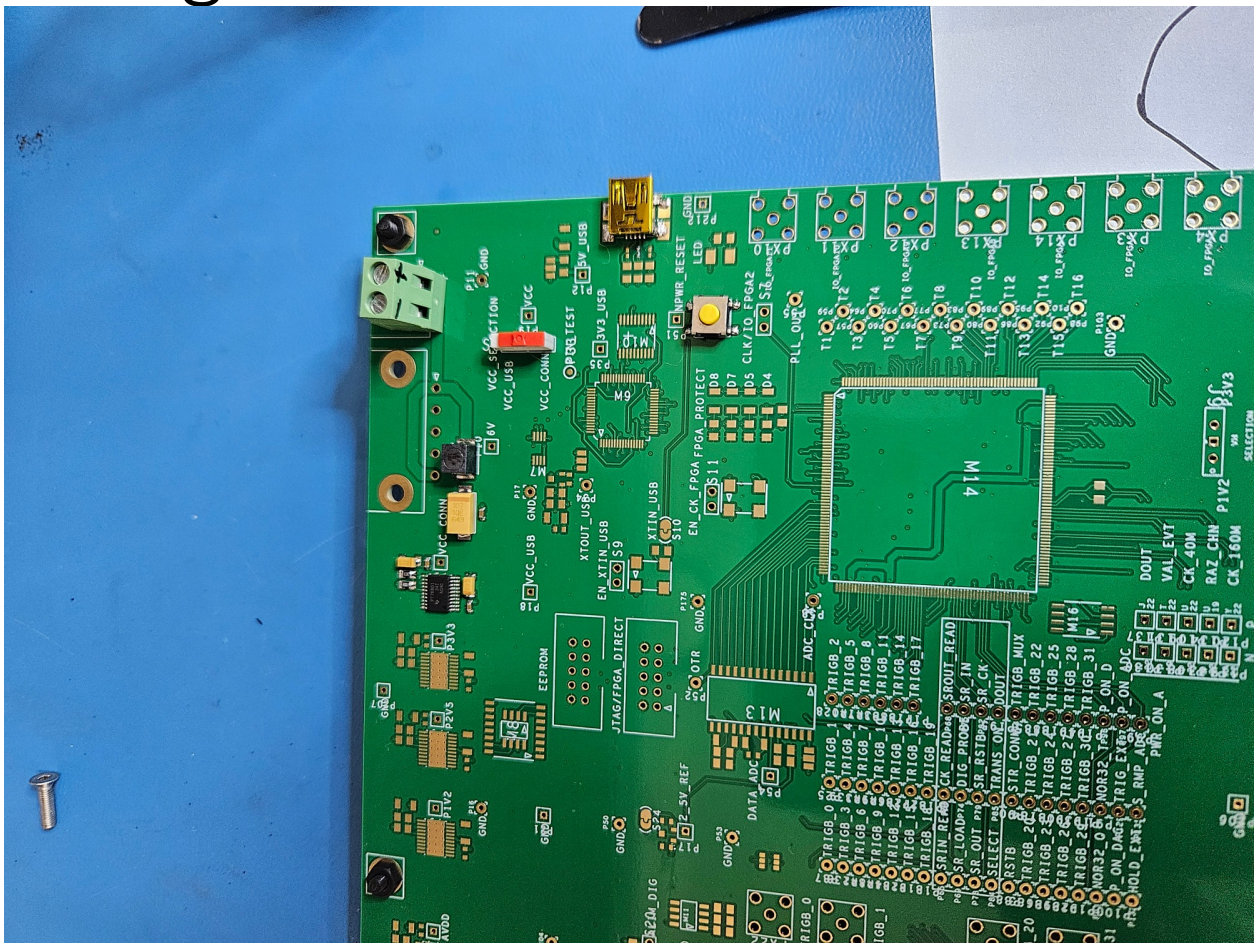
8-layers
PCB

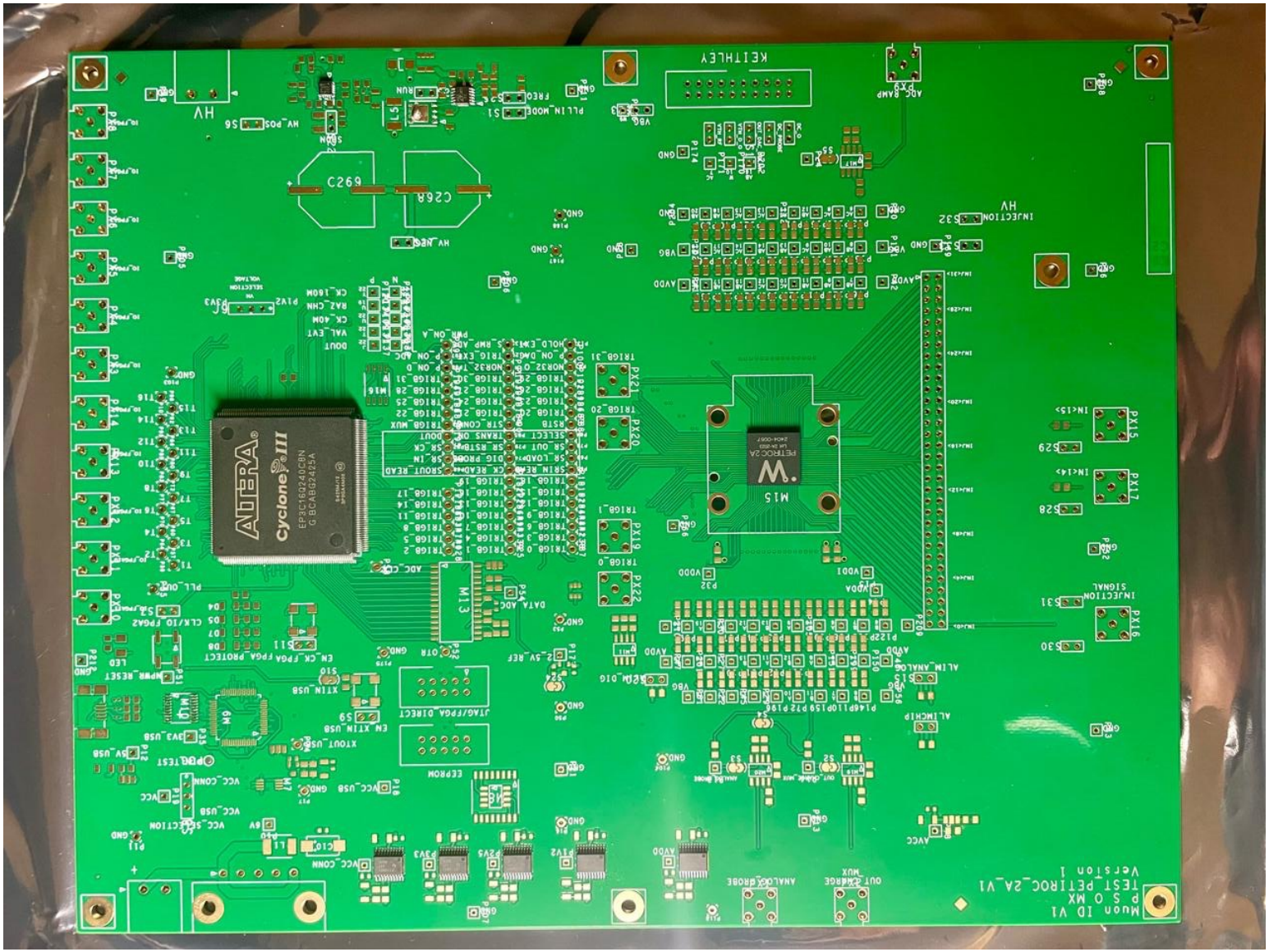


Petiroc 2A
Footprint



Power Regulator Test





Placement of Critical Components

Verifications

- Power Connectors -> OK
- Blind Vias -> OK
- Power regulators:
  - 1-> 3.3V -> OK
  - 2-> 3.3V -> OK
  - 3-> 5V -> OK
  - 4-> 1.2V -> OK
  - 5-> 3.3 V usb -> OK
  - 6-> 2.5V -> OK
- VSS -> OK
- VDD1 -> OK
- VDDA -> OK
- VDDD -> OK
- AVDD -> OK

- CLK 40 MHz-> OK
- CLK 12MHz -> OK
- EPC FPGA -> OK
- ADC9220 -> OK
- Temp Sensor1 -> 0%
- Temp Sensor 2 -> 0%
- Memory -> 0%
- USB comm-> 0%
- PETIROC 2A -> 30%
  - Inputs -> ok
  - Outputs -> 0%
  - Config -> 0%
- FPGA –> 25%
- HV_POS –> 25%
- HV_NEG –> 25%

PCB assembly

- Mexico -> CERN: 9 Nov
- CERN service to solder Petiroc, FPGA and 8 Power Reg.
- PCB return to Mexico: Nov 28
- Complete:
  - Power Regultors
  - FPGA components
  - USB chips and components
- Last part: HV Pos and Neg

First TEST (December 2024)

Documentation is in progress

- USB Communication
- FPGA Communication
- PETIROC 2A Communication and configuration

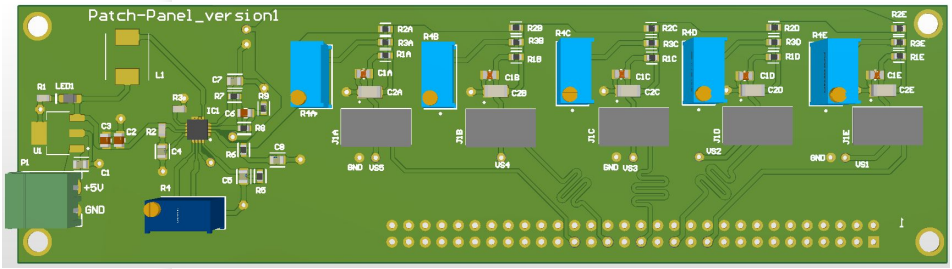
- Start General Configuration

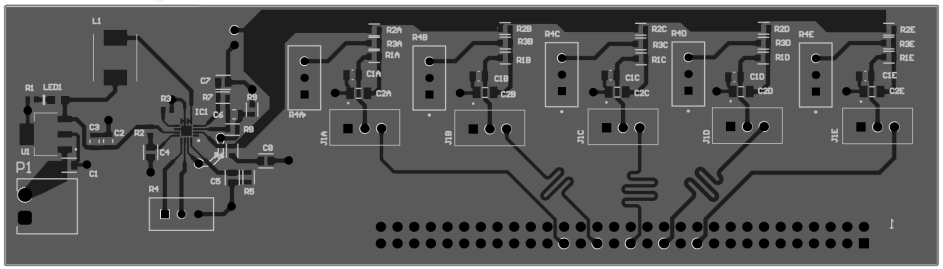
- Test Data transfer

- Test general response with function Generator

Patch Pannel (V1)

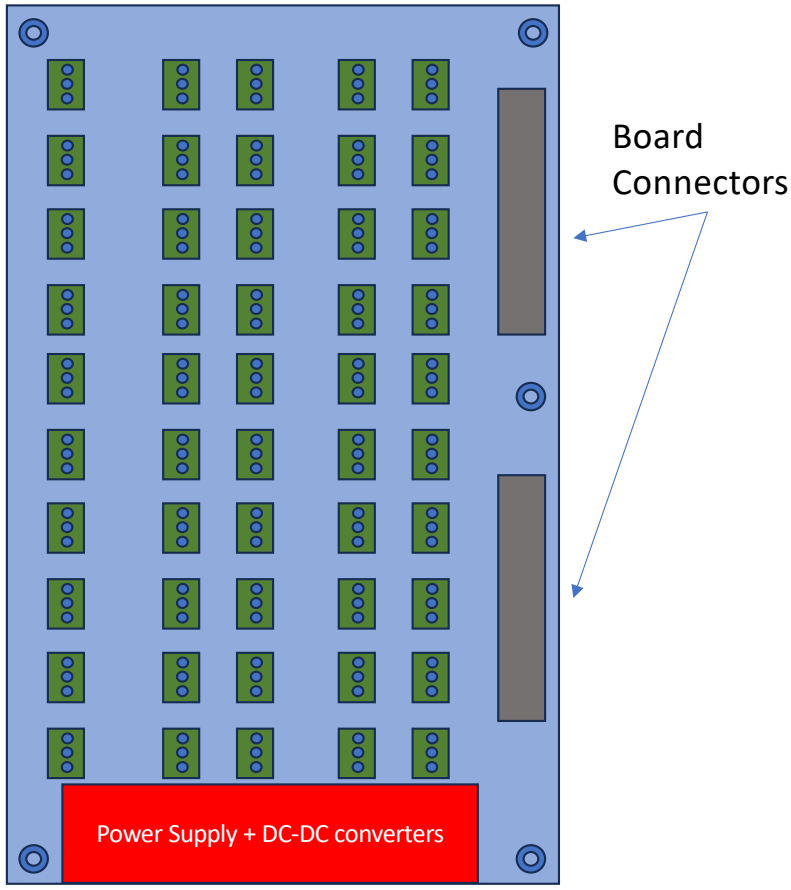
- 5 Channels PCB completed
- Power regulator included in PP for 5 SiPM
- To test Power regulator, noise and signal integrity
- -Amplification stage for RPCs





Patch Pannel (V2)

- 50 Channels
- Upgrade of the first patch pannel version
- Schematic is in progress



User Interface

- Compatible with Weeroc Test Board
- Working on start procedure:
  - Connnects USB cable
  - Power up power supply
  - Start Software
- Slow Control:
  - Load slow control parameters
  - 640 bits will be sent twice

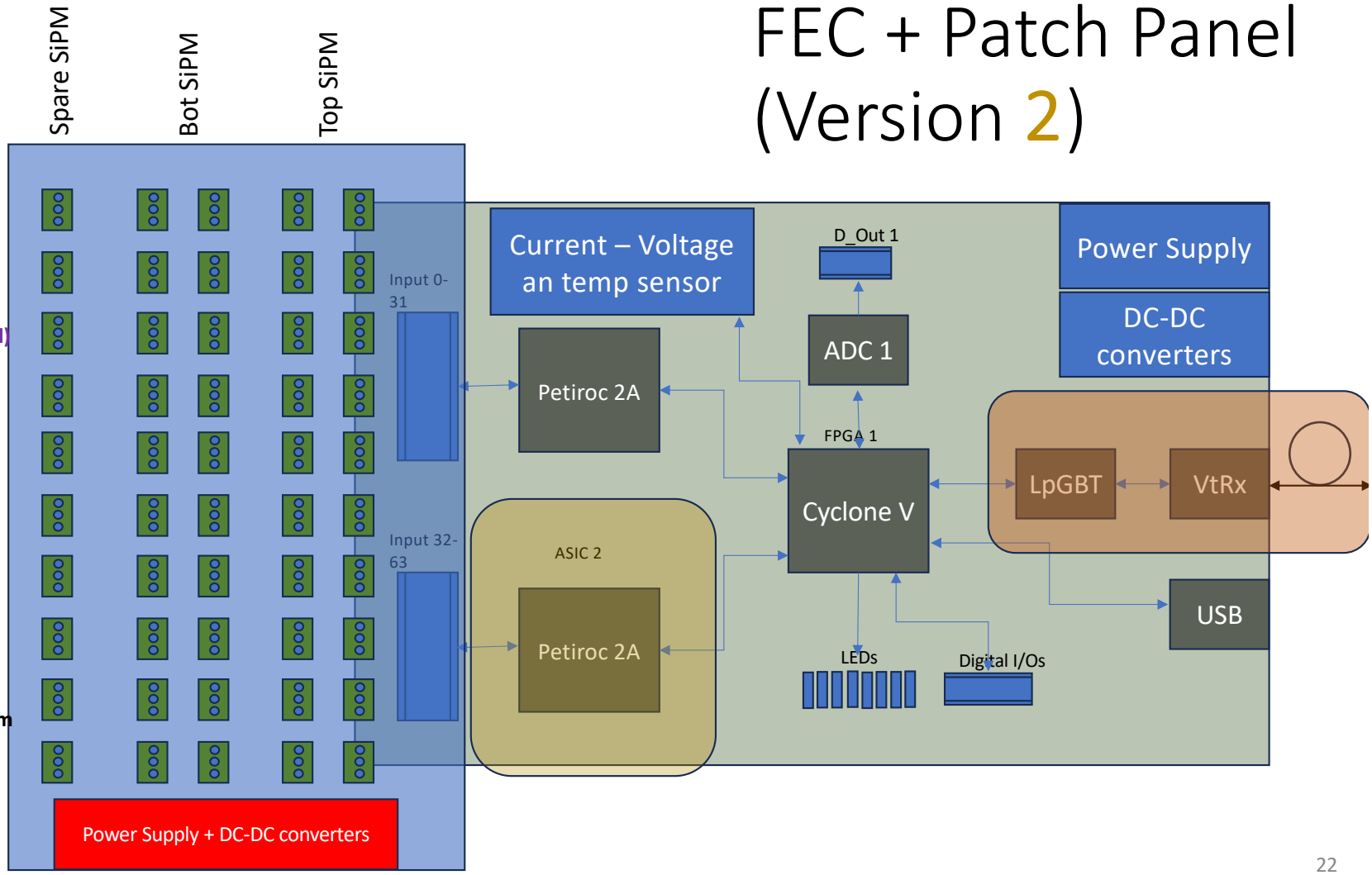
- Calibration:
  - Calibrate the 6-bits DAC settings of each channel
- Data Acquisition:
  - Number of acquiisitions
  - Trigger mode (under revision)
  - Output file and format
- Preparing technical documentation
  - Manual FEC
  - Manual Interface

Radiation Tolerances

- FEC located in a region with a “moderate” radiation dose estimated by simulations.
- Not negligible for our FPGA. We are still investigating different ways for a save operation.
- FEC will be tested under radiation sources to observe aging effects or SEU.

FEC + Patch Panel (Version 2)

- 2 ASIC Petiroc 2A
- 1 FPGA Cyclone V (non Rad-Hard 5cgtfd5c5f23c7n)
- 1 LpGBT + VtRx+ (for communication and Slow control)
- USB communication for debugging
- 50 Channels input
- Charge and Time measurements
- Channel by channel SiPM high voltage adjustment
- 6mW/channel power consumption
- PP connectors –> header 1.28 mm
- Version 2 -> 2025



Muon ID Electronics group

- Sinaloa
  - Carlos Duarte Galvan
  - Juan Manuel Mejia Camacho
  - Cesar Regalado Elenes
  - Juan Carlos Cabanillas Noris
- UNAM
  - Enrique Patiño Salazar
  - Saul Aguilar
- Puebla
  - Emigdio Jimenez Dominguez
  - Yael Antonio Vazquez Beltrán
  - Guillermo Tejeda Muñoz

- Luis A. Pérez Moreno

FEE
Grafic Interface

SiPM

PCB FEC
Patch Panel
Firmware

Communication protocols

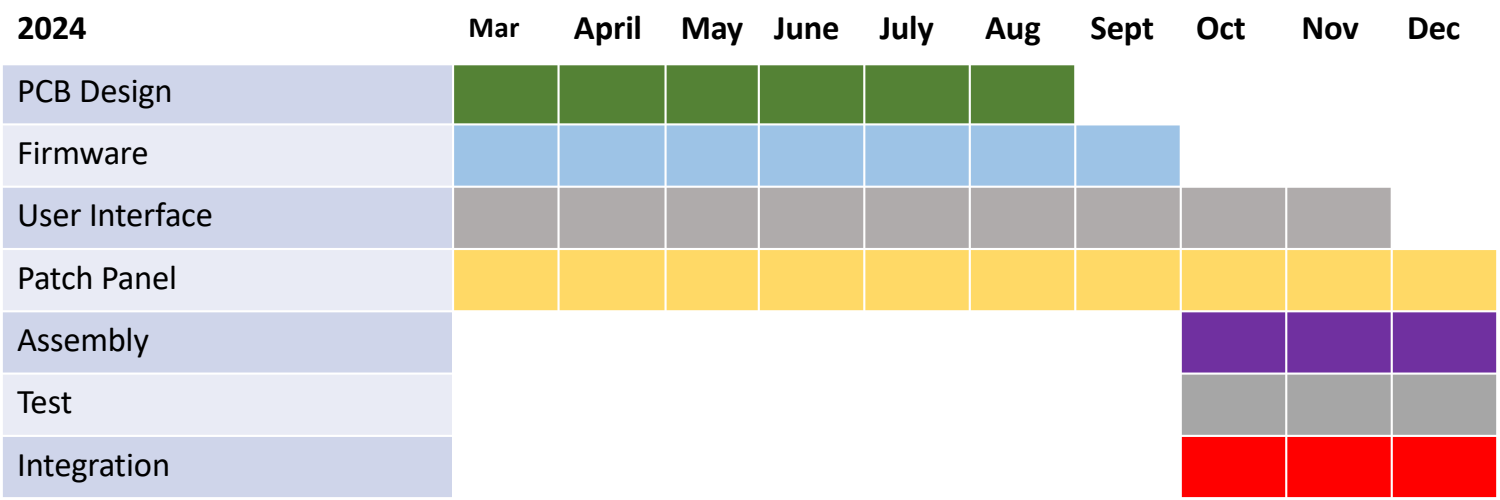
Bi weekly meeting for preparation of the electronics proposal and TDR

Summary

- MuonID FEC Version 1-> Design finished and in construction.
- User interface for first tests is completed.
- Integration to Muon Id modules in 2025
- First tests with cosmic rays in 2025
- Test Beam in summer 2025
- Muon ID FEC Version 2 design completed in 2025

Thank You for your attention

Time Line (FEC Version 1)



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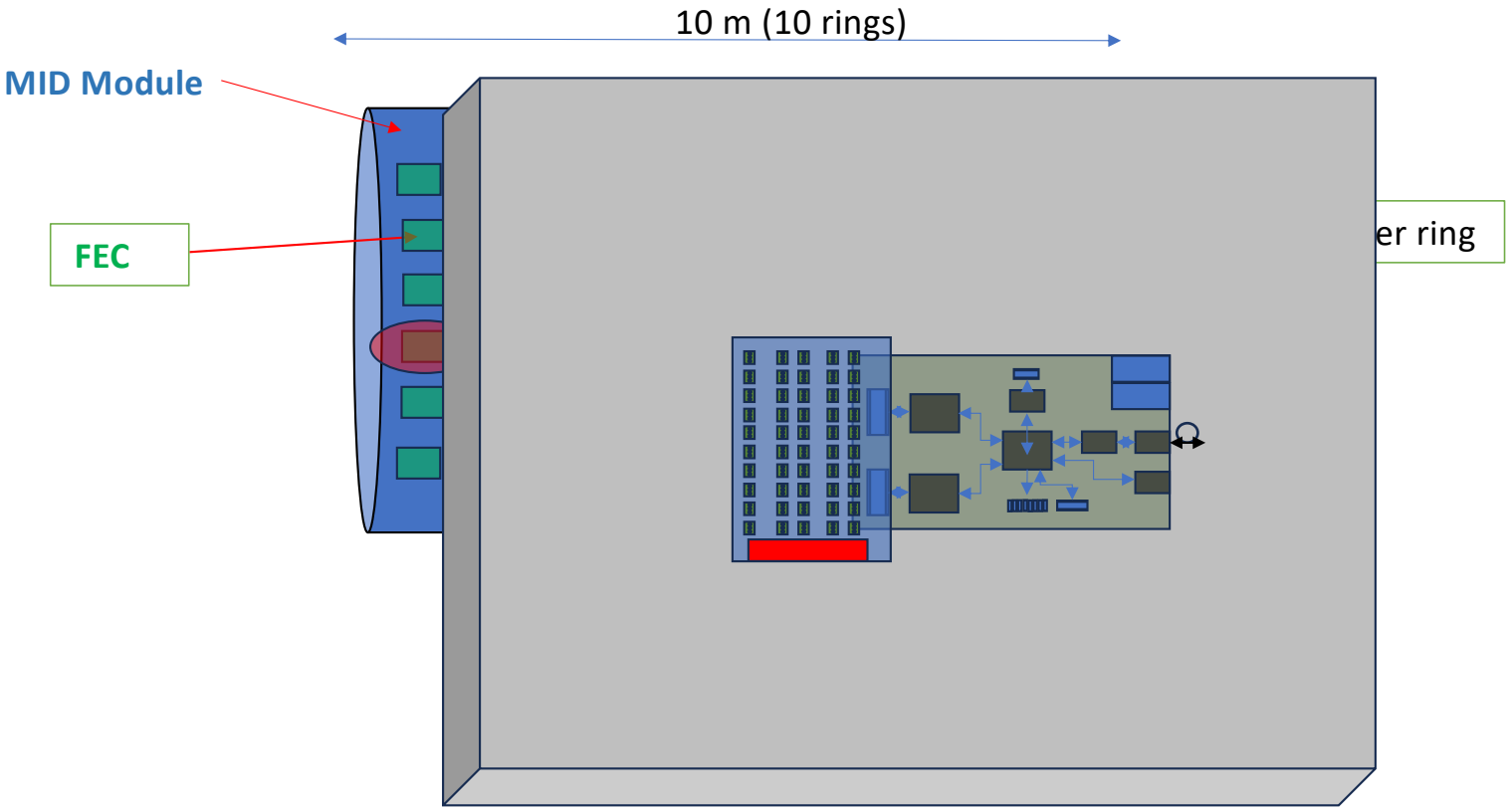

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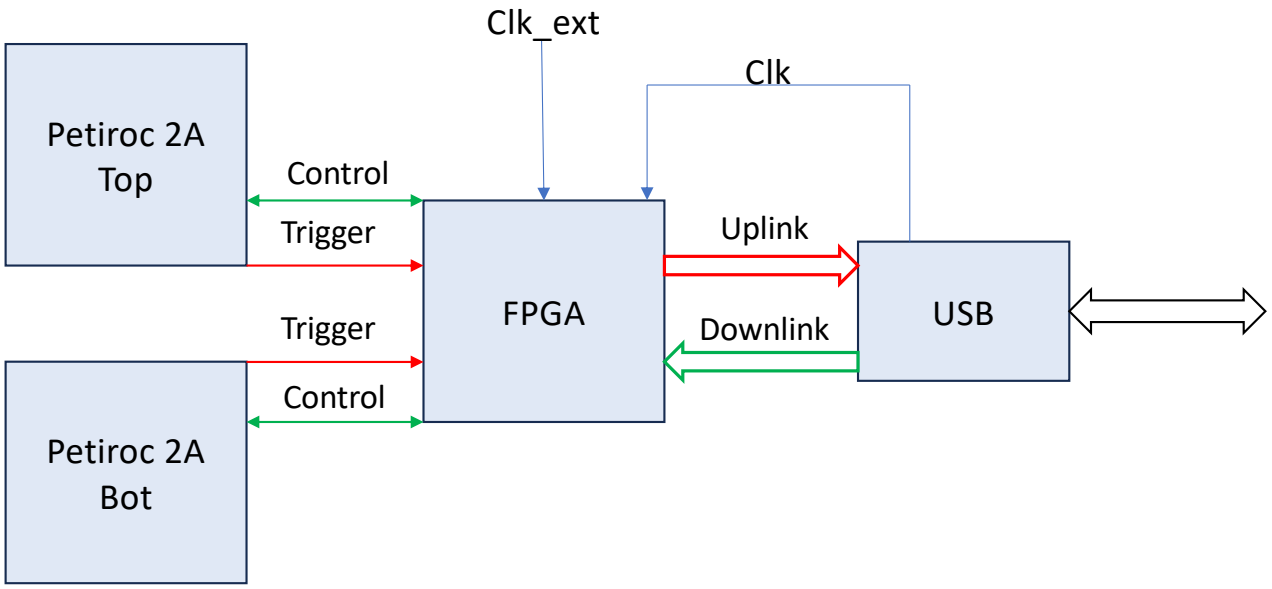
MuonID FEC details



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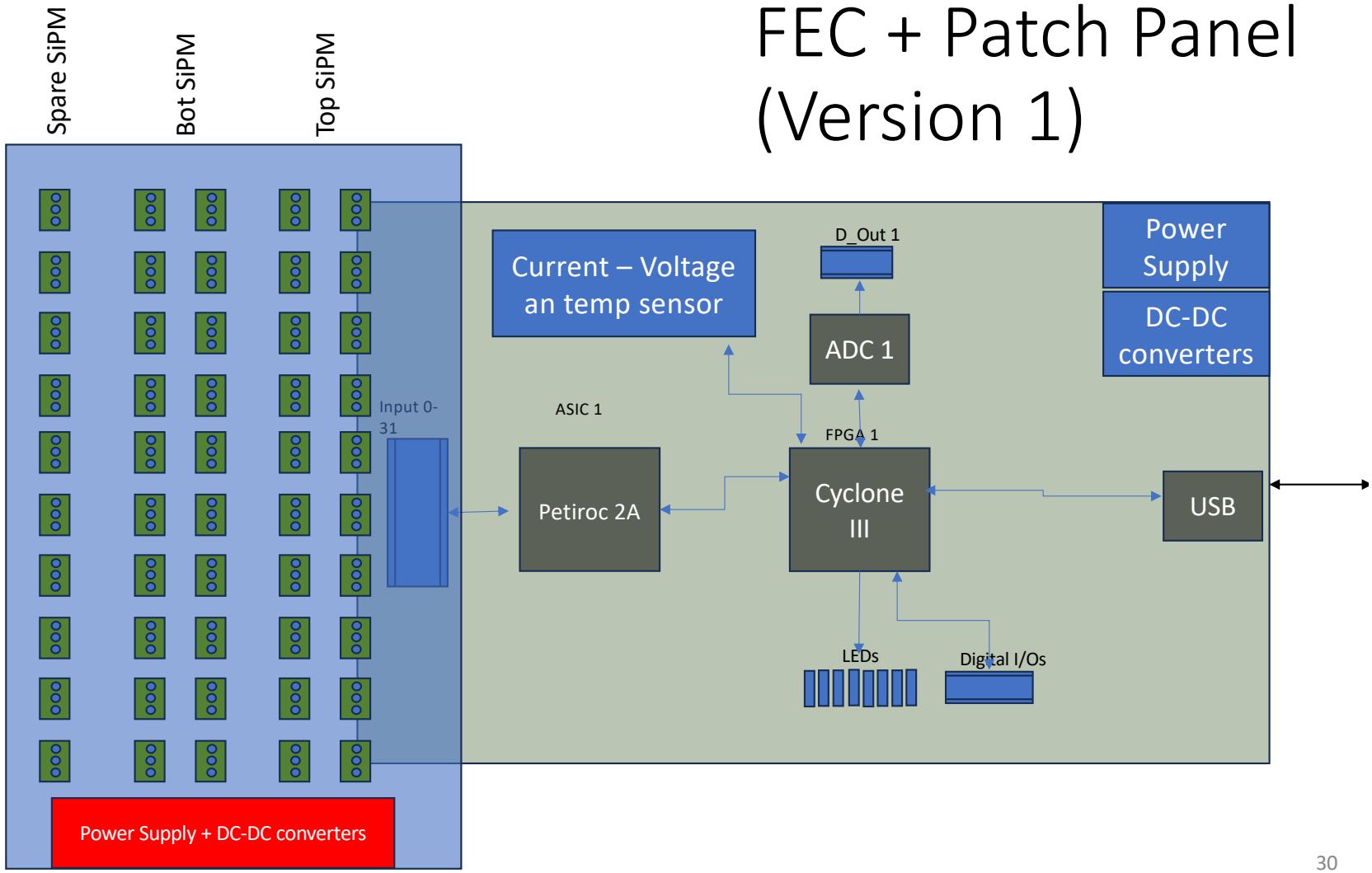
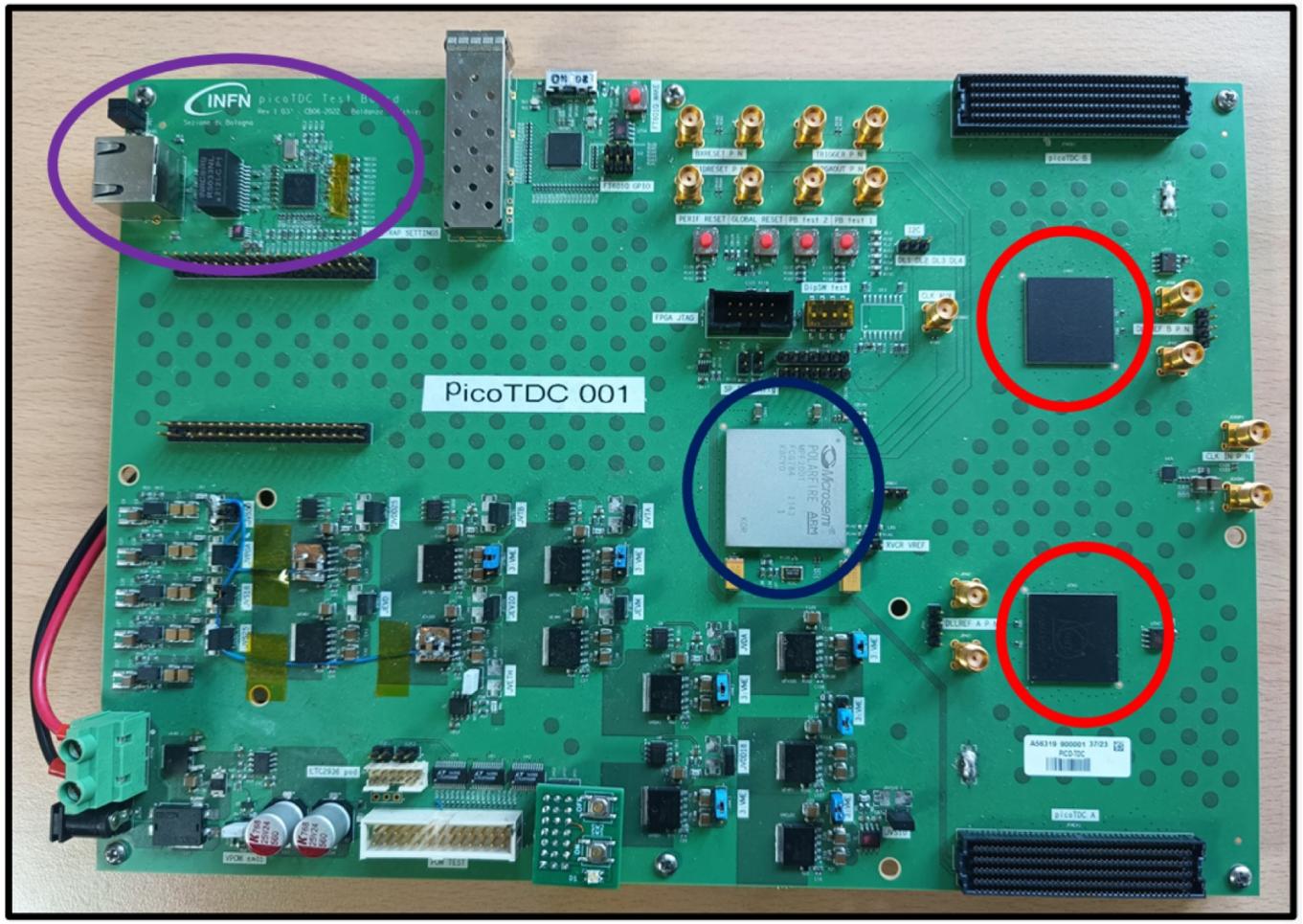


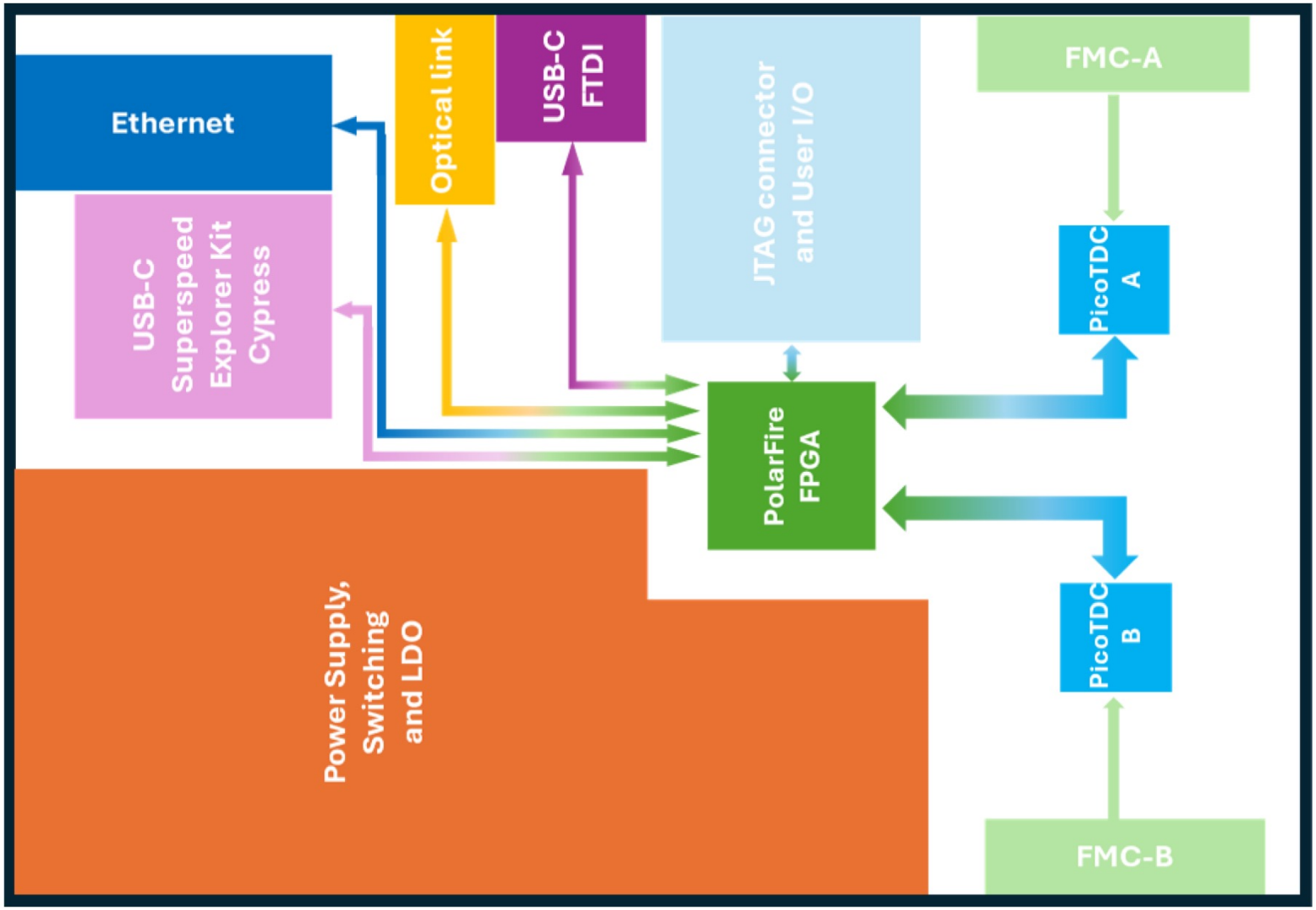
TOF design

PicoTDC board
PolarFire FPGA (blue)
2 PicoTDCs (red)
Ethernet connector subsystem (purple)



- FPGA based design

- PolarFire MPF200T FCG784E



Dose tolerances (from CMS)

- TID (γ´s):
  - FPGA Cyclone V (50Gy)
  - Petiroc 2A (160Gy)
  - Power Regulators (100Gy)
- TNID (Neutrons):
  - 25e11 neq1MeV/cm^2
- Neutron flux:
  - 450e3 neq1MeV/cm^2/s

SEU expected in FPGA

Expected fluence and dose (MID zone):

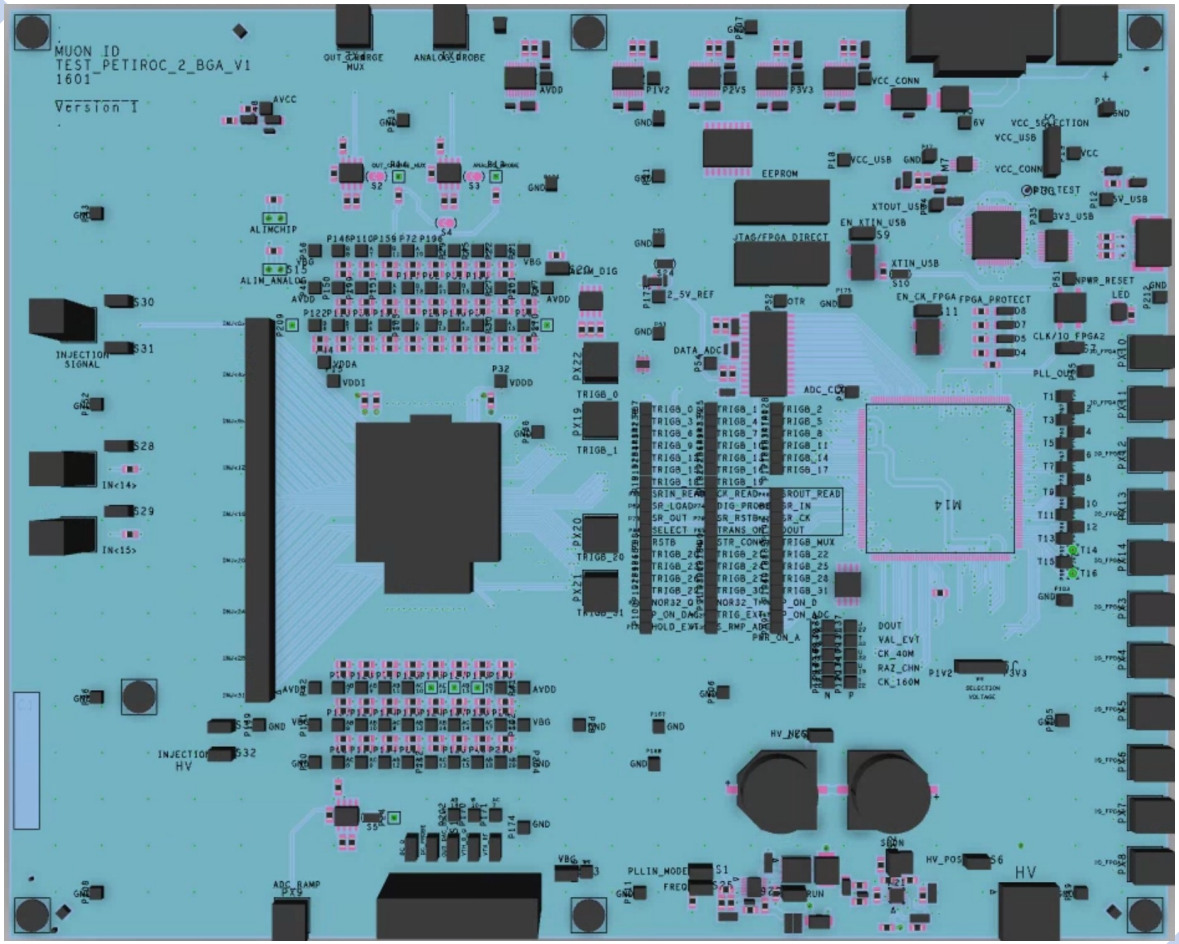
Radiation load for Run 5+6 in the MID

	R = 301 cm	
	pp	**Pb-Pb**
TID (rad)	54	0.94
NIEL (1 MeV neq/ cm^2)	3.4×10^{10}	4.7×10^{8}
HEH (Hz/cm^2)	17	4.3
Ch. particle fluence rate (Hz/cm^2)	3.6	1.1

Table 3. Radiation load in the MID simulated with FLUKA considering ***Run 5+6 period and assuming a running efficiency of 65%.***

25 cm

20 cm



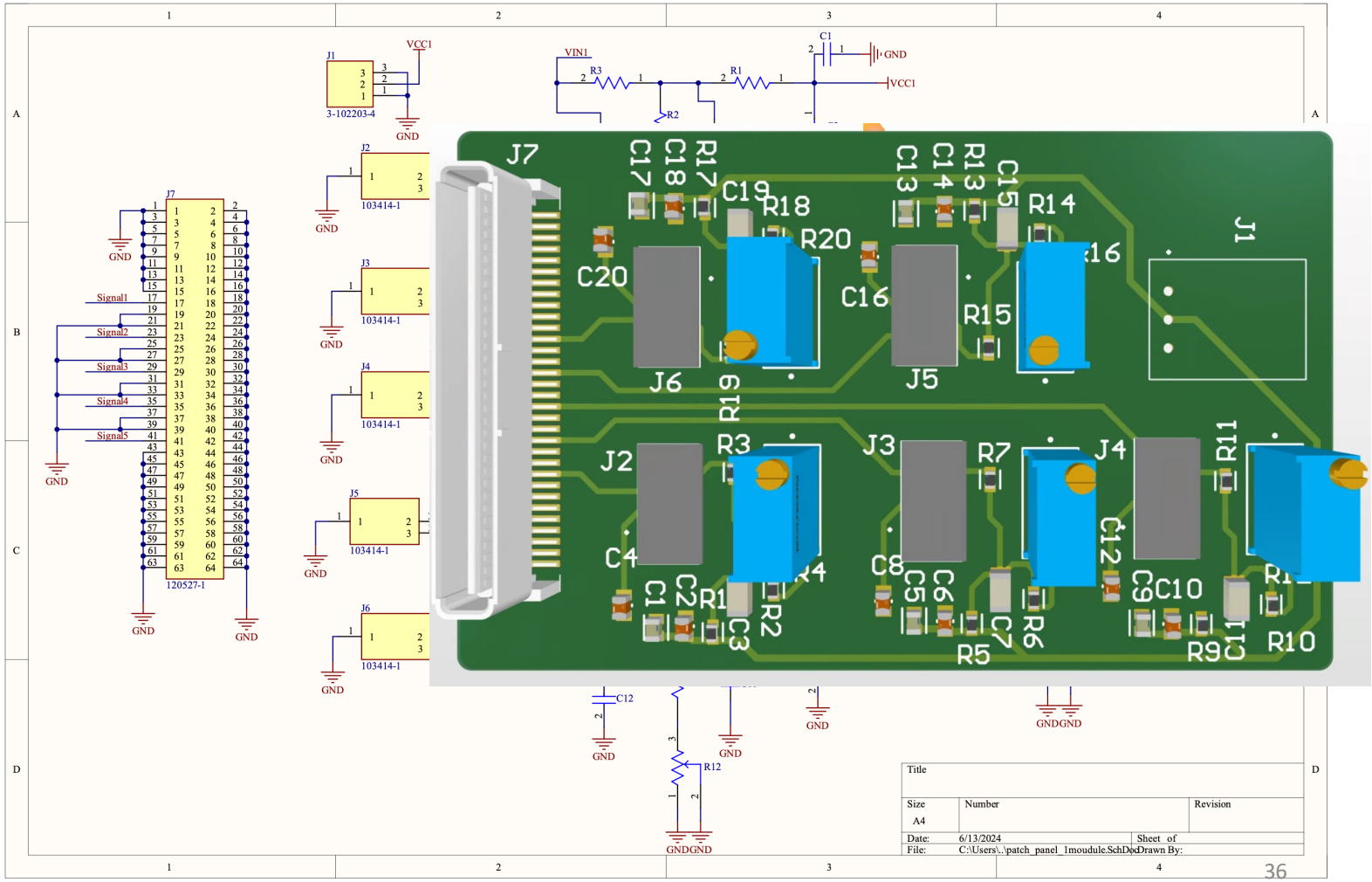
-Design Rule Check (ok)
-Gerber Files
-8 layers
-32 Channels
-USB communication

-80% parts available

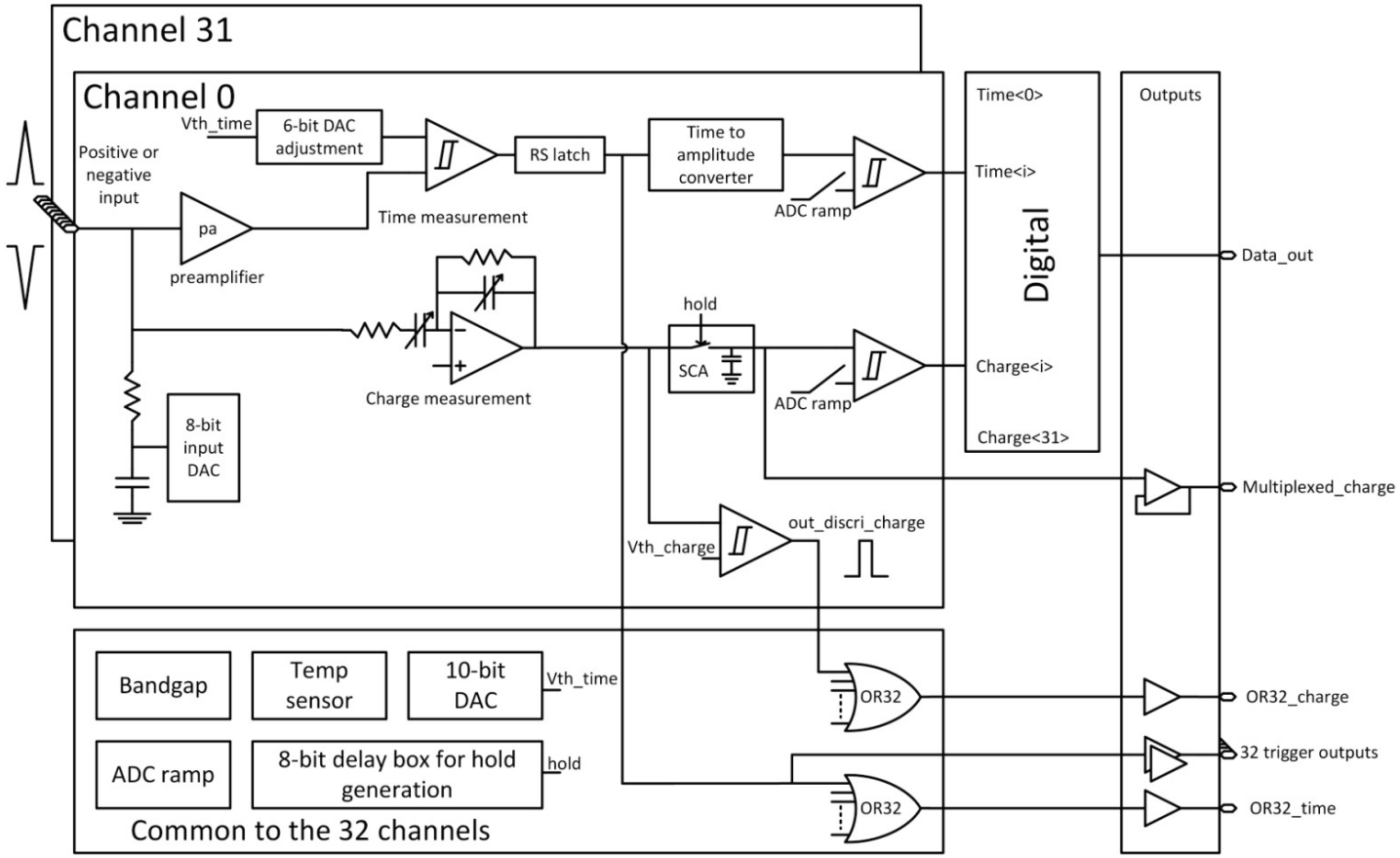
Recuerde que tiene que considerar una PCB para destrucción junto con un chip.

Patch-Panel Schematic Partial

First version to test:
Crostalk
Noise
Stability



Petiroc 2A


Channel 31
Channel 0
Vth_time
6-bit DAC adjustment
Positive or negative input
pa
preamplifier
Time measurement
RS latch
Time to amplitude converter
ADC ramp
Time<0>
Time<i>
Digital
Charge<i>
Charge<31>
Outputs
Data_out
hold
SCA
Charge measurement
8-bit input DAC
Multiplexed_charge
Vth_charge
out_discri_charge
Bandgap
Temp sensor
10-bit DAC
Vth_time
OR32
OR32_charge
ADC ramp
8-bit delay box for hold generation
hold
32 trigger outputs
OR32_time
Common to the 32 channels

Specifications

Detector Read-Out	SiPM, SiPM array
Number of Channels	32
Signal Polarity	Positive or Negative
Sensitivity	Trigger on first photo-electron
Timing Resolution	~ 35 ps FWHM in analogue mode (2pe injected) - ~ 100 ps FWHM with internal TDC
Dynamic Range	3000 photo-electrons (10^6 SIPM gain), Integral Non Linearity: 1% up to 2500 ph-e
Packaging & Dimension	TQFP208 – TFBGA353
Power Consumption	Power supply: 3.3V 192mW Analogue core (excluding analogue outing buffer), 6mW/ch
Inputs	32 voltage inputs with DC adjustment for SiPM HV tuning
Outputs	Digital output (energy on 10 bit, time on 10 bit - 40ps bin) 32 trigger outputs 1 multiplexed charge output, 1 multiplexed hit register 2 ASIC trigger outputs (Trigger OR on 32 channels, 2 levels)
Internal Programmable Features	32 HV adjustment for SiPM (32x8b), trigger threshold adjustment (10b), charge measurement tuning, 32 trigger masks, internal temperature sensor, trigger latch