

# MiniBeBe Detector

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Concept and Status

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01

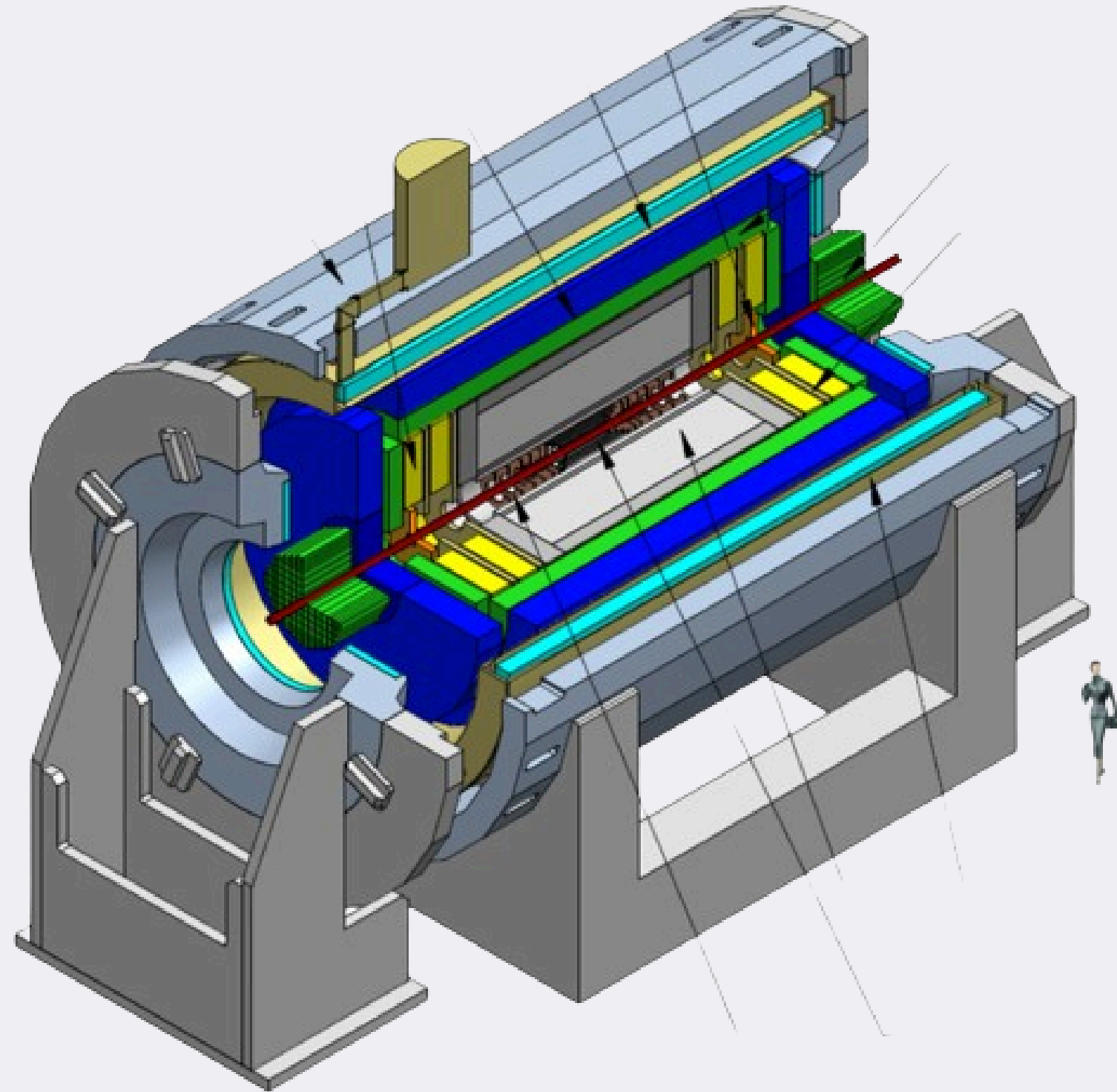
# MiniBeBe

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Current Concept



# MPD



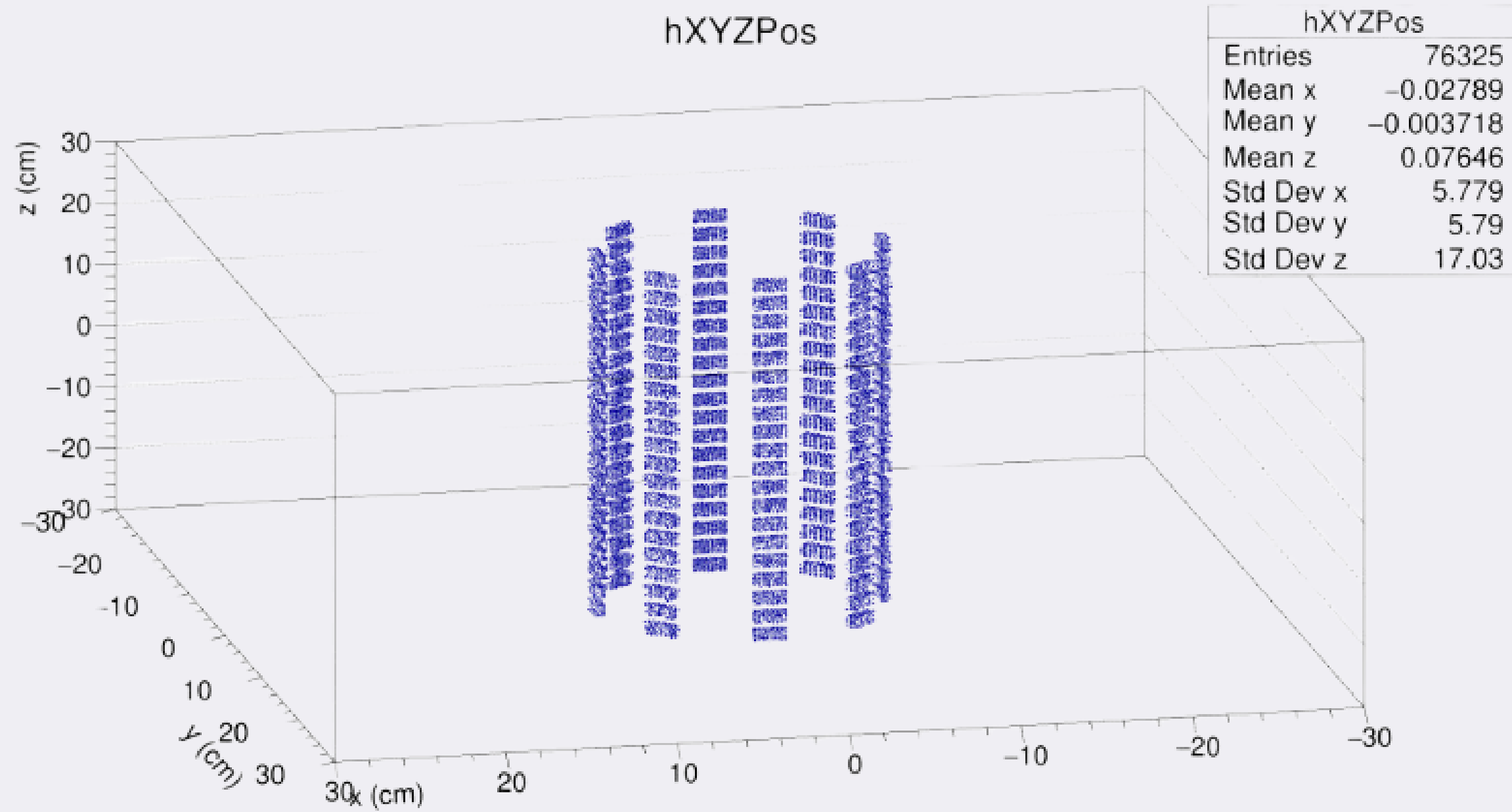
- Originally proposed as a wake up trigger for TOF
- Demanded efficient detection capabilities for low multiplicities  $p+p$ ,  $p+A$  and  $A+A$  events
- Several adjustments in its design
- Adapted to the mechanical support of ITS
- Designed to be used only in Phase 0



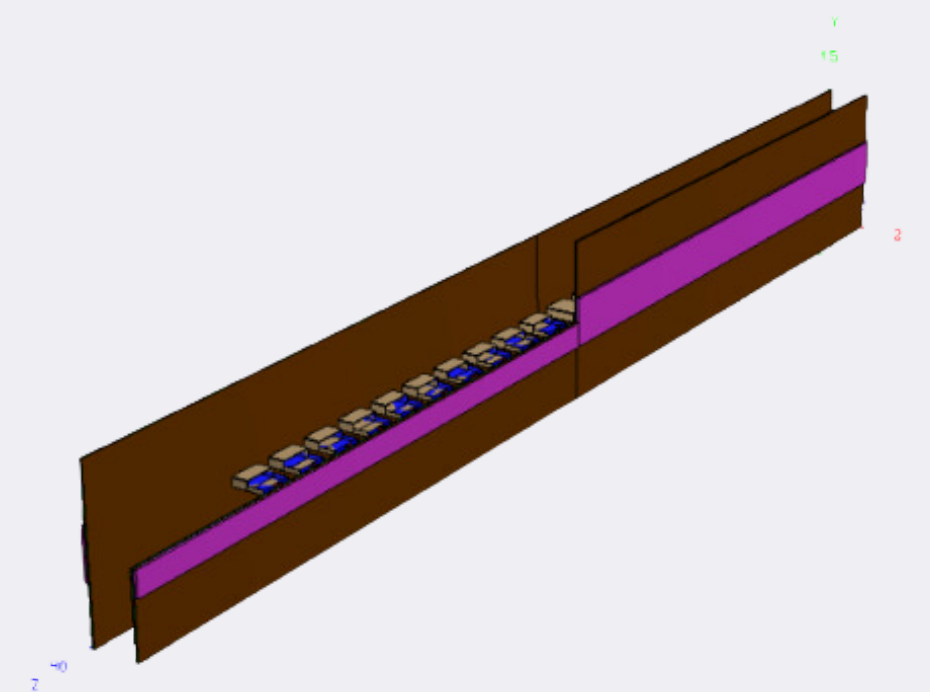
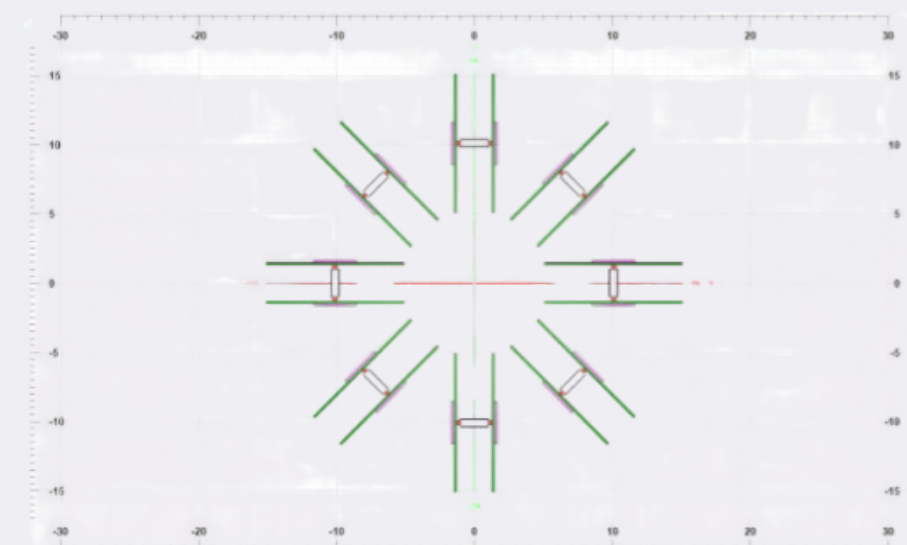
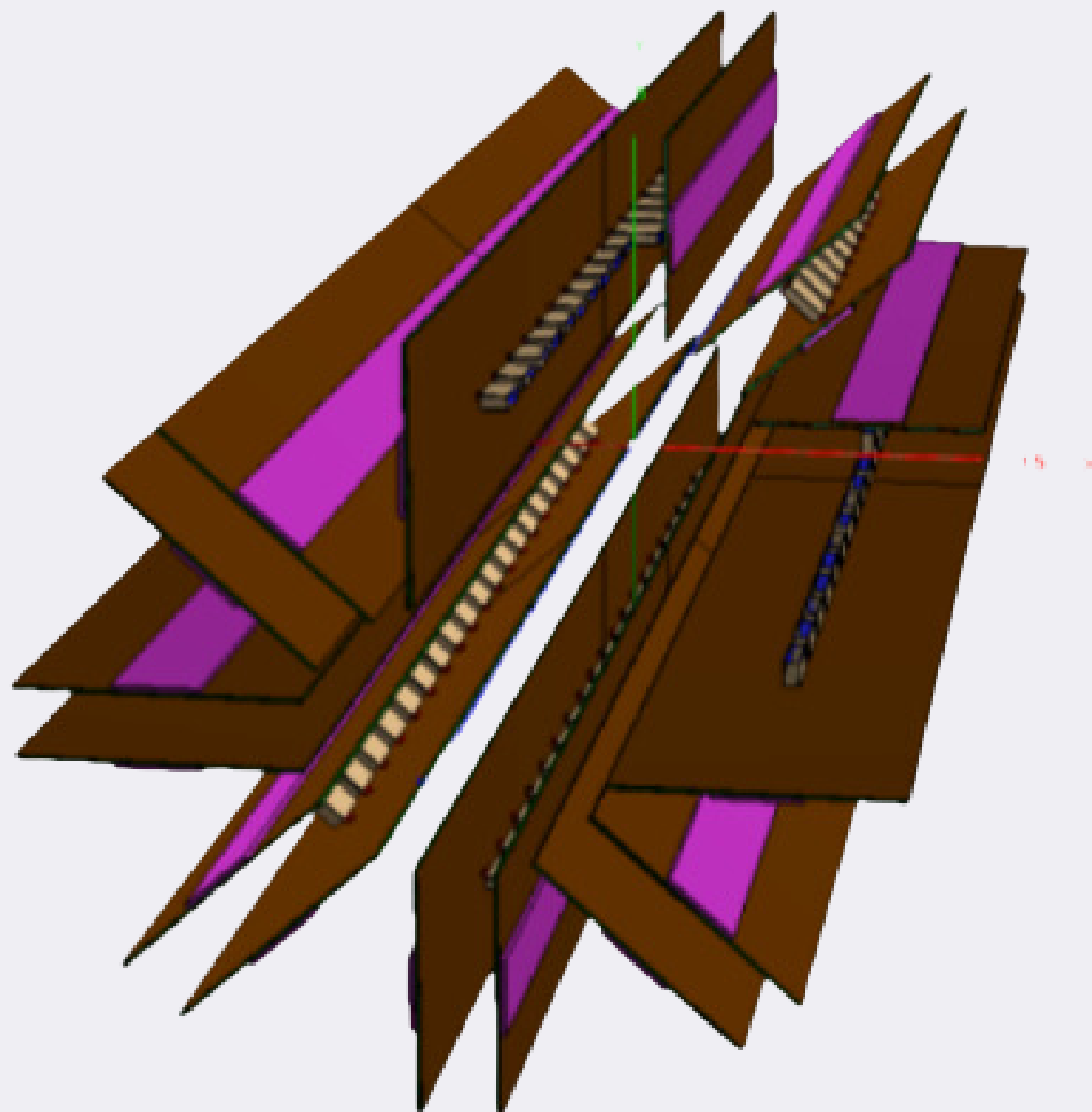
# MiniBeBe

- 8 **H-shaped** rails
- Each module is formed by
  - A cuboid of **20 plastic scintillators** (EJ232, 20x20x5mm<sup>3</sup>)
  - Each plastic surrounded by **two SiPM** (Hamamatsu Series 13, area 3.07x3.07mm<sup>2</sup>) and electronics at each side
  - Fixed between the PCB and the Cold Plates
  - Electronic boards of 80-100mm width, ~100mm length
  - Cold Plates are the same of ITS
- Same space as ITS

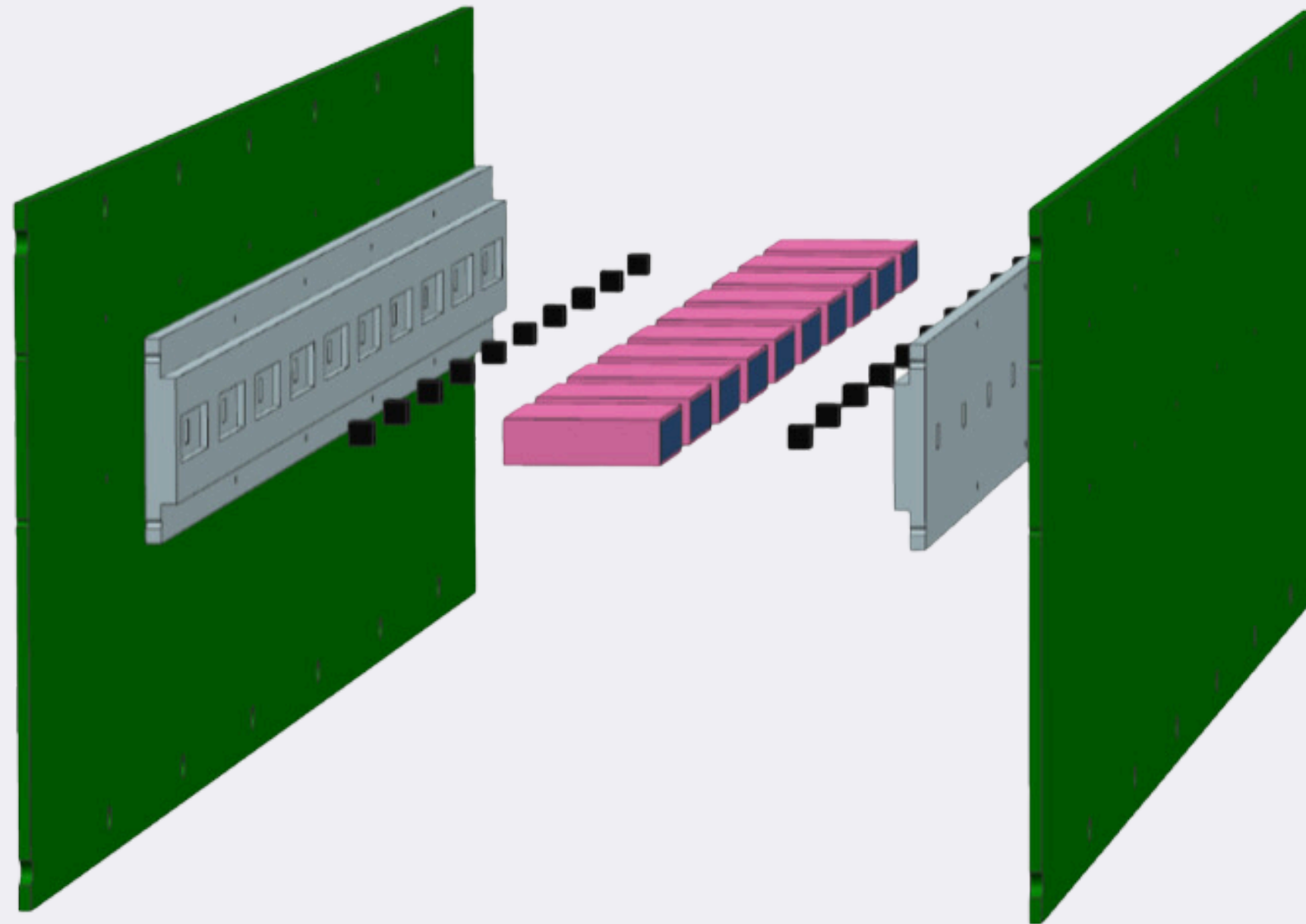
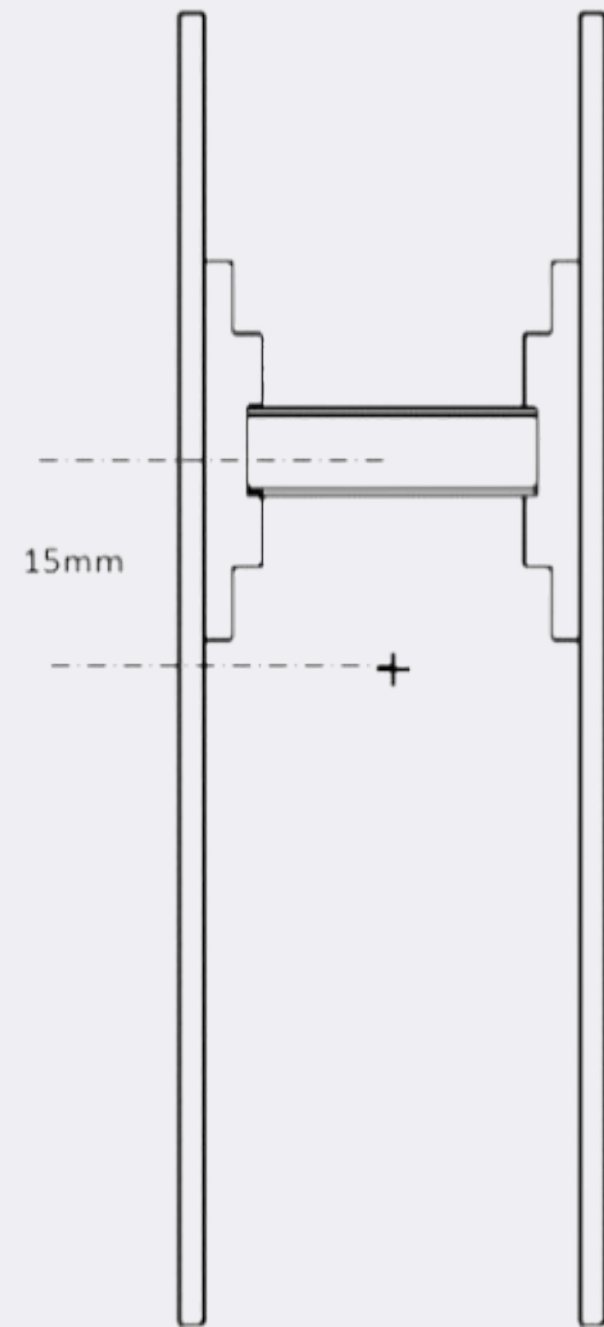
# MiniBeBe



# MiniBeBe



# MiniBeBe





02

# Mechanics

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Plug & Play MPD-ITS Mechanical Support

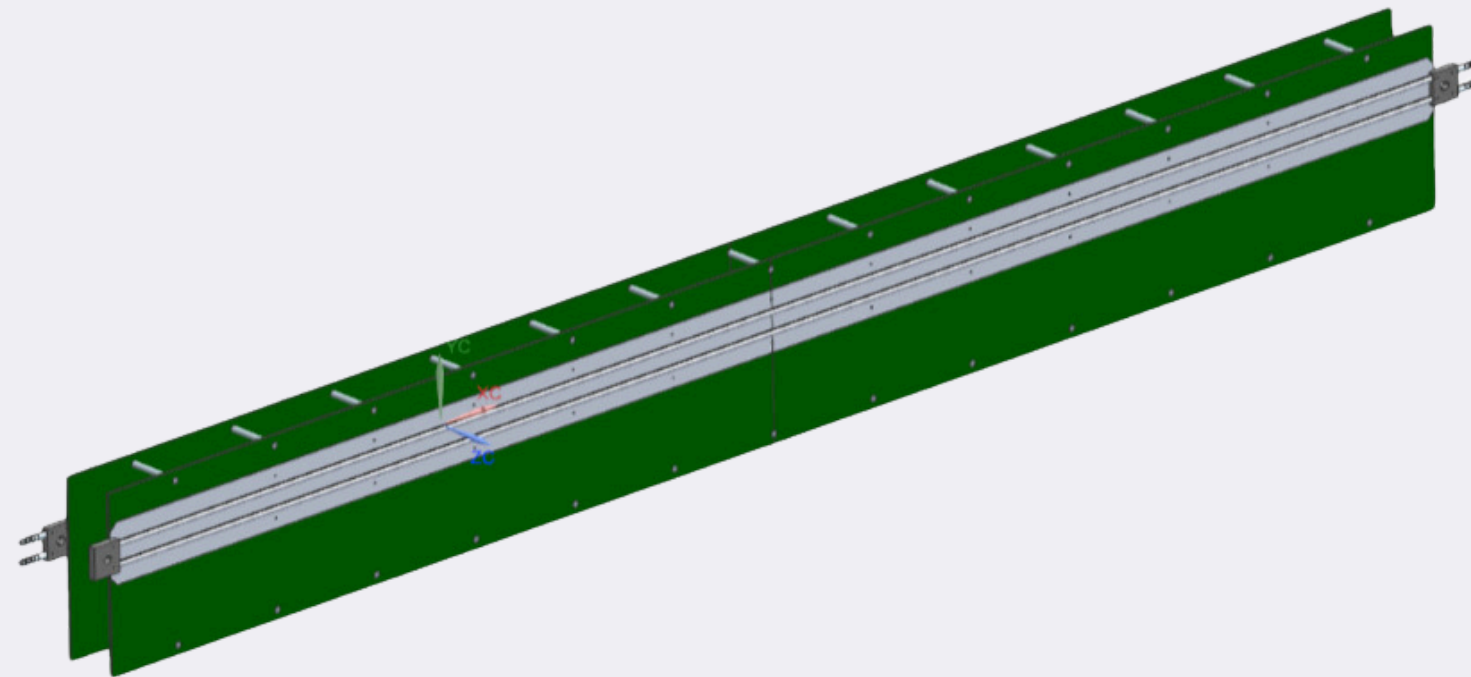


# Restrictions

- Adapt to the ITS detector general housing
- Not to use magnetic materials
- Avoid the creation of shadow
- Minimal material budget
- Maximal number of modules

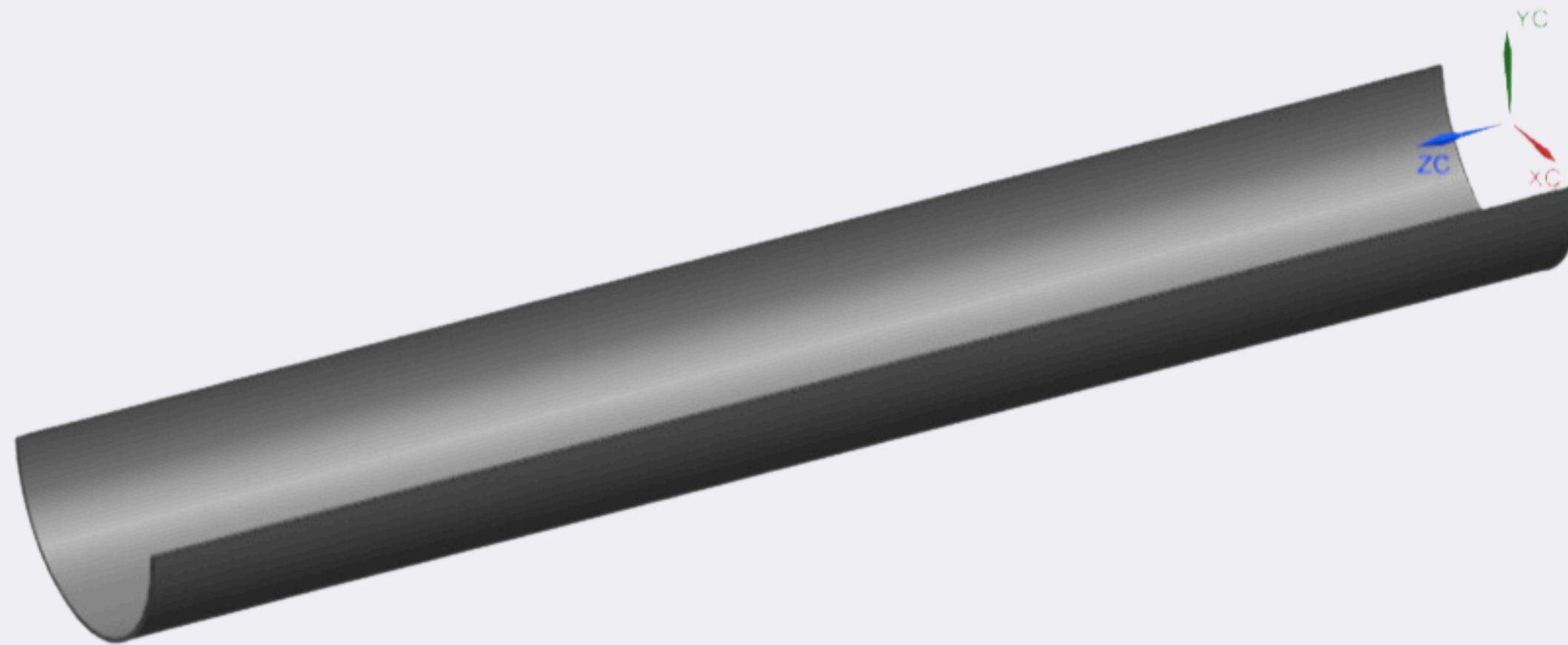
# Design

- Housing at 312mm
- Maximum 8 modules, 8-10mm width
- Same cooling system as ITS



# Design

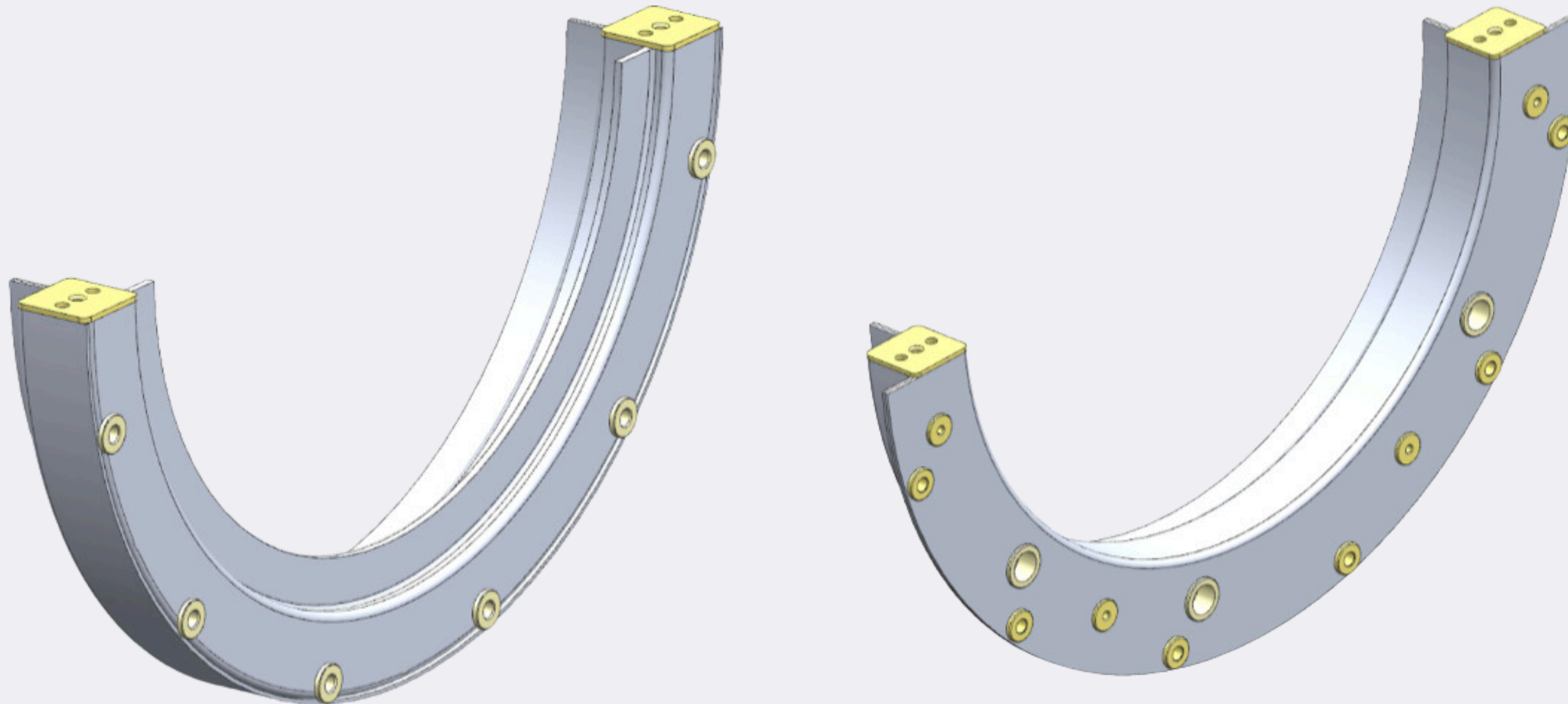
- Plug & Play with ITS
- Housing in the 3rd and 4th layers of ITS
- 312mm in diameter, 161mm in length





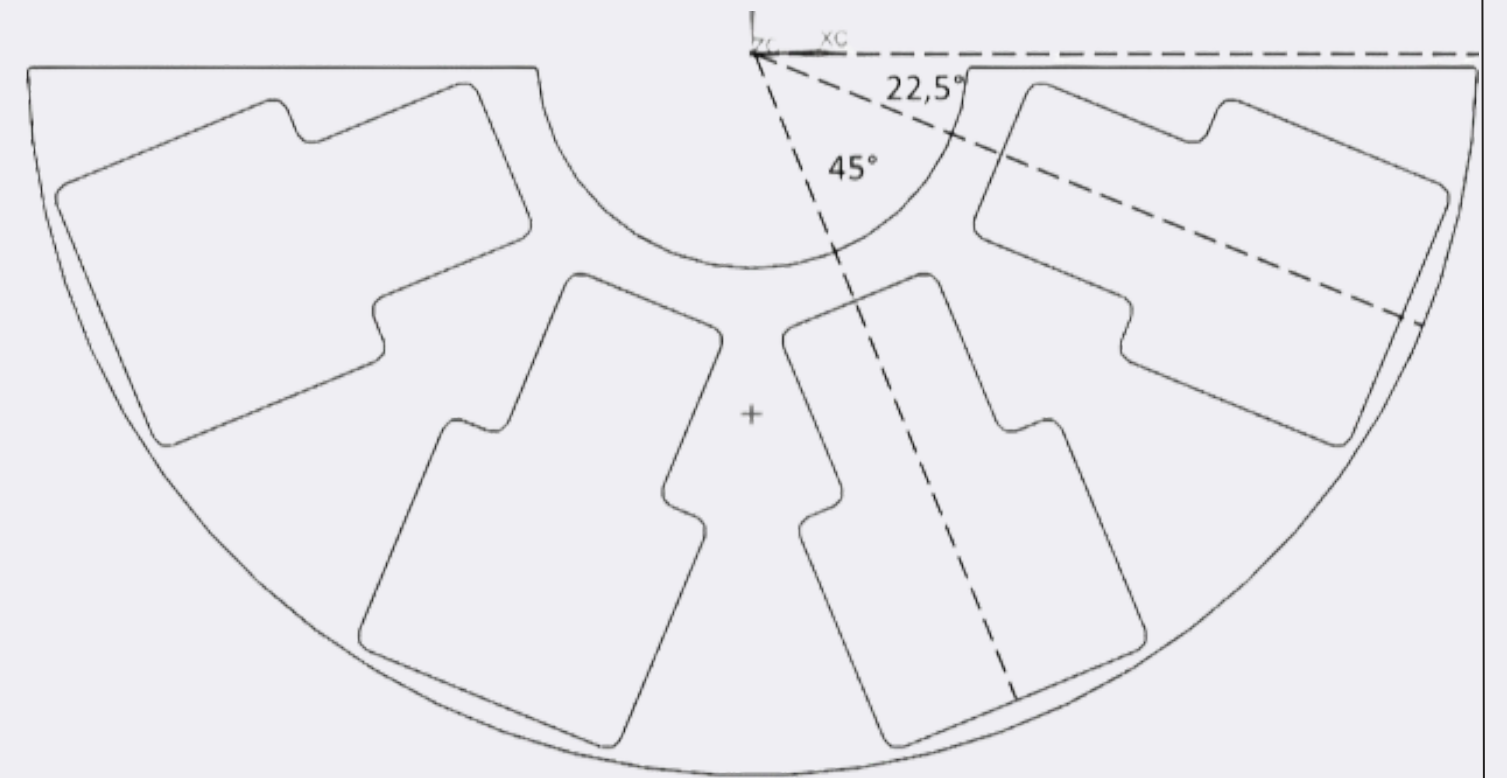
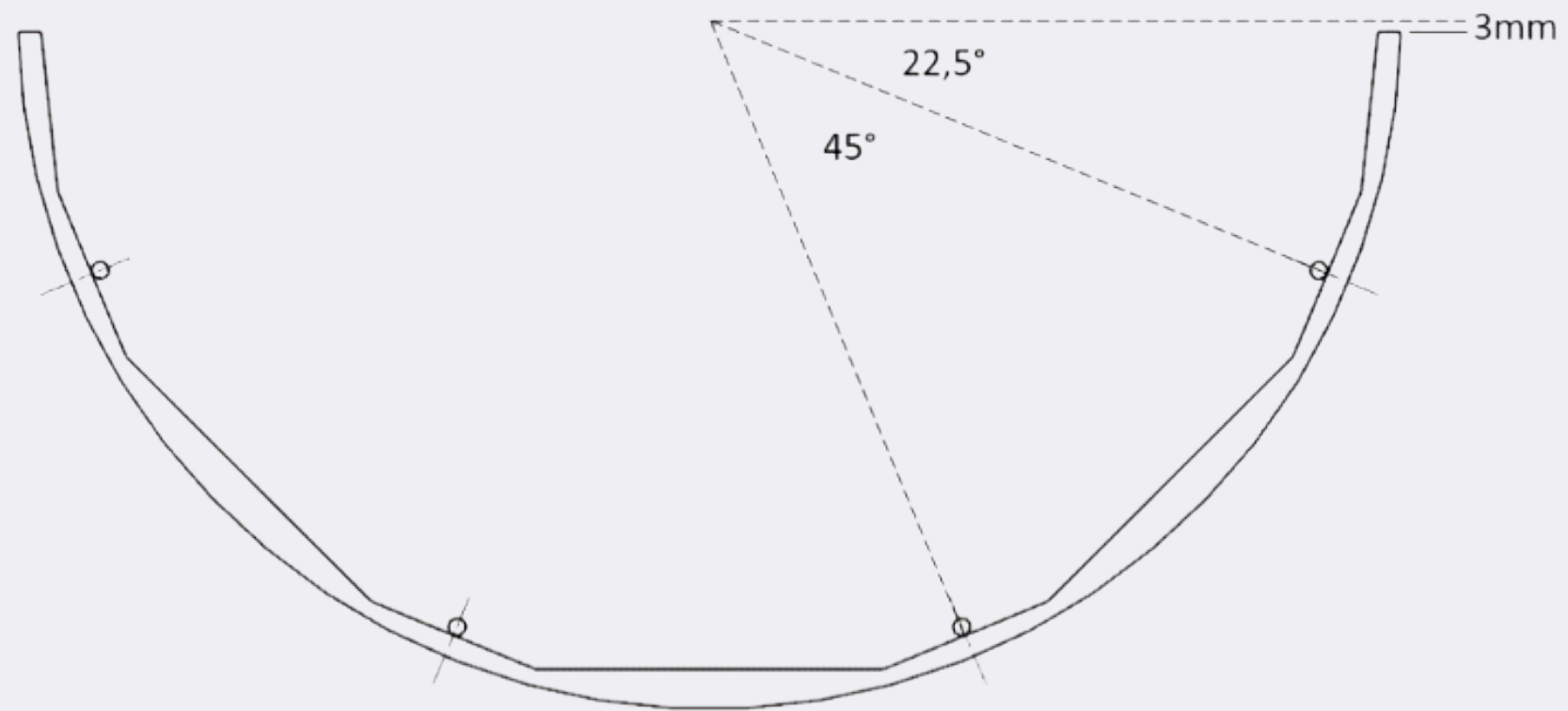
# Design

- Flanges of the 4th layer of ITS were redesigned
- Bushings of 9.3mm



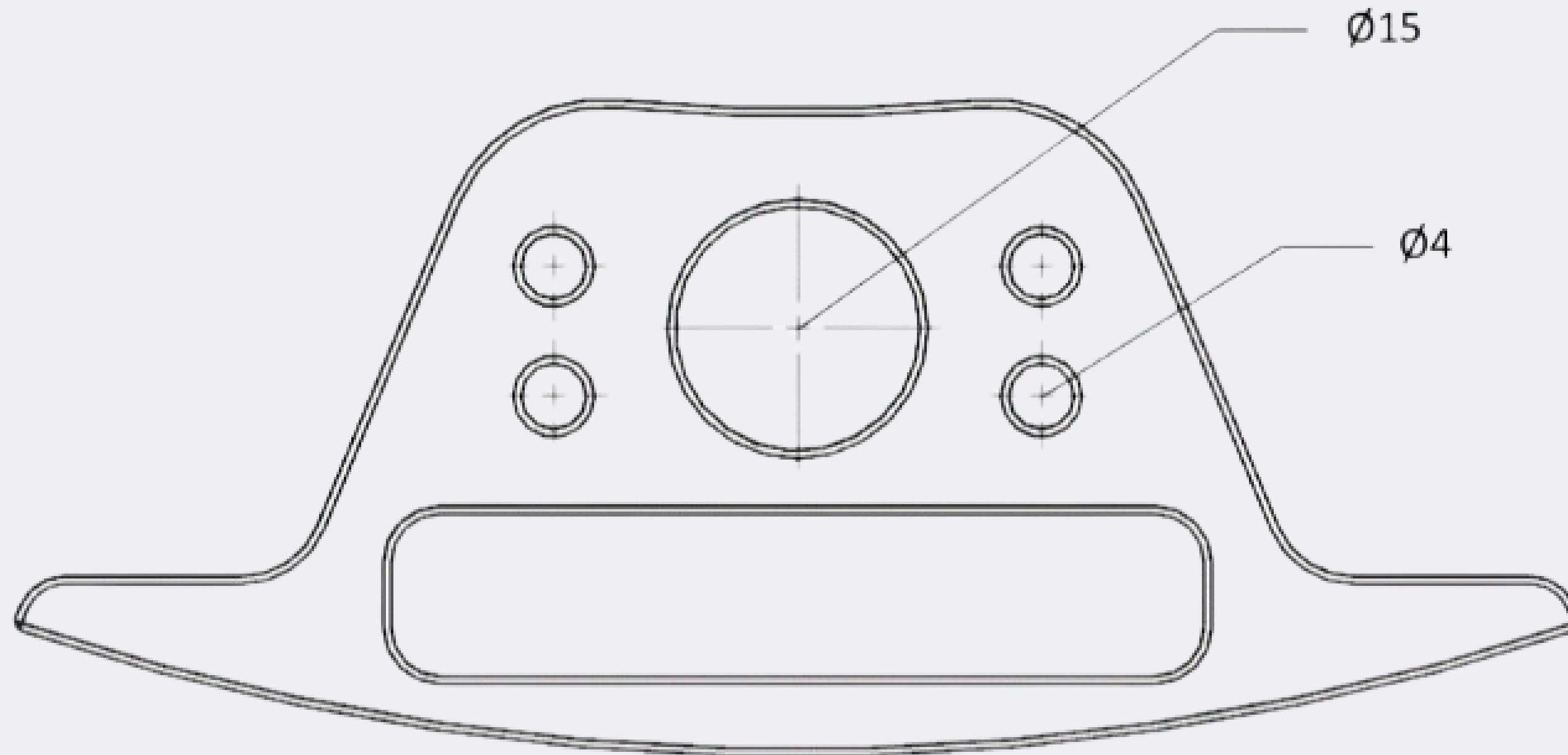
# Design

- Electronic modules fixed with flanges



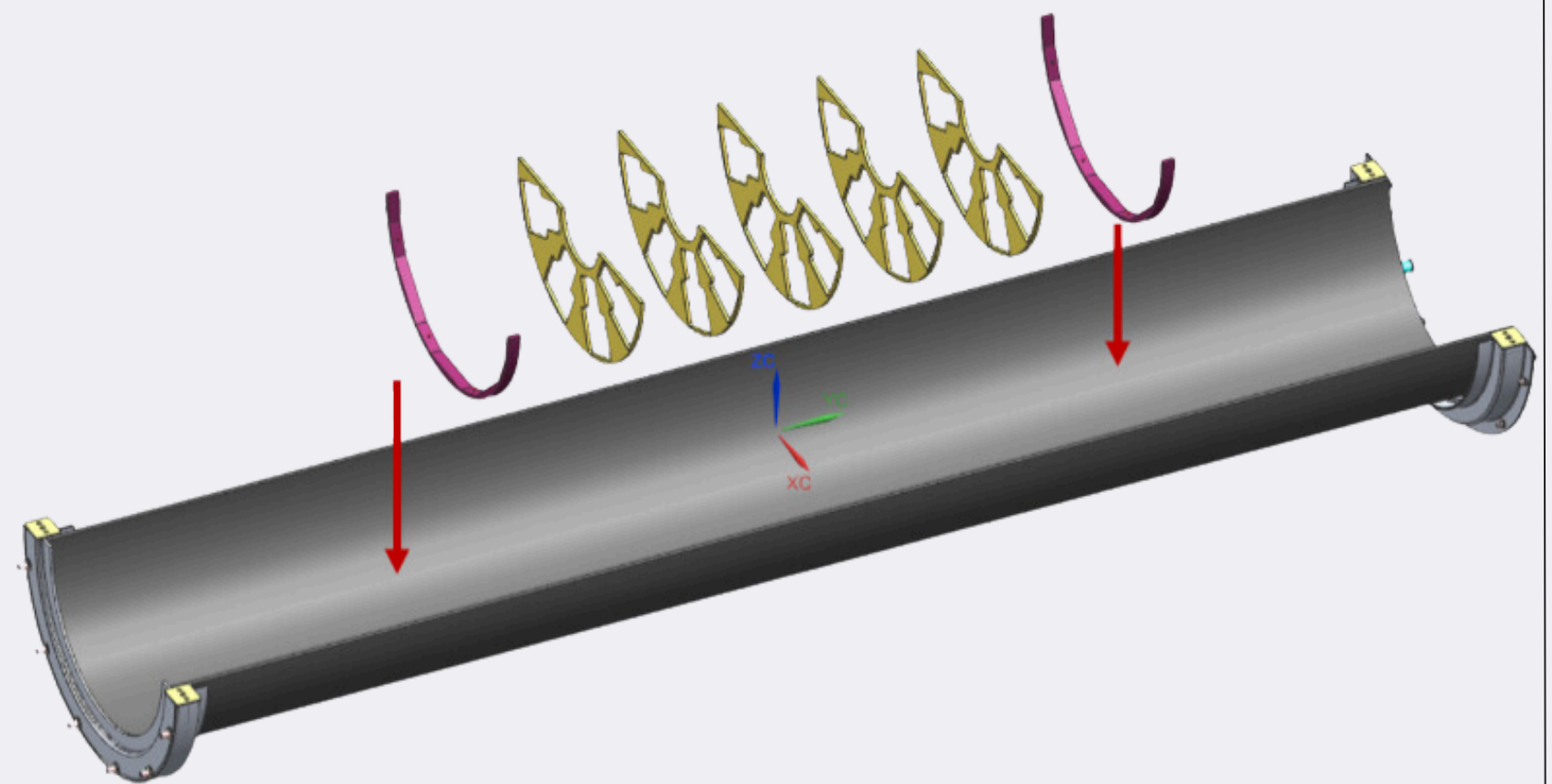
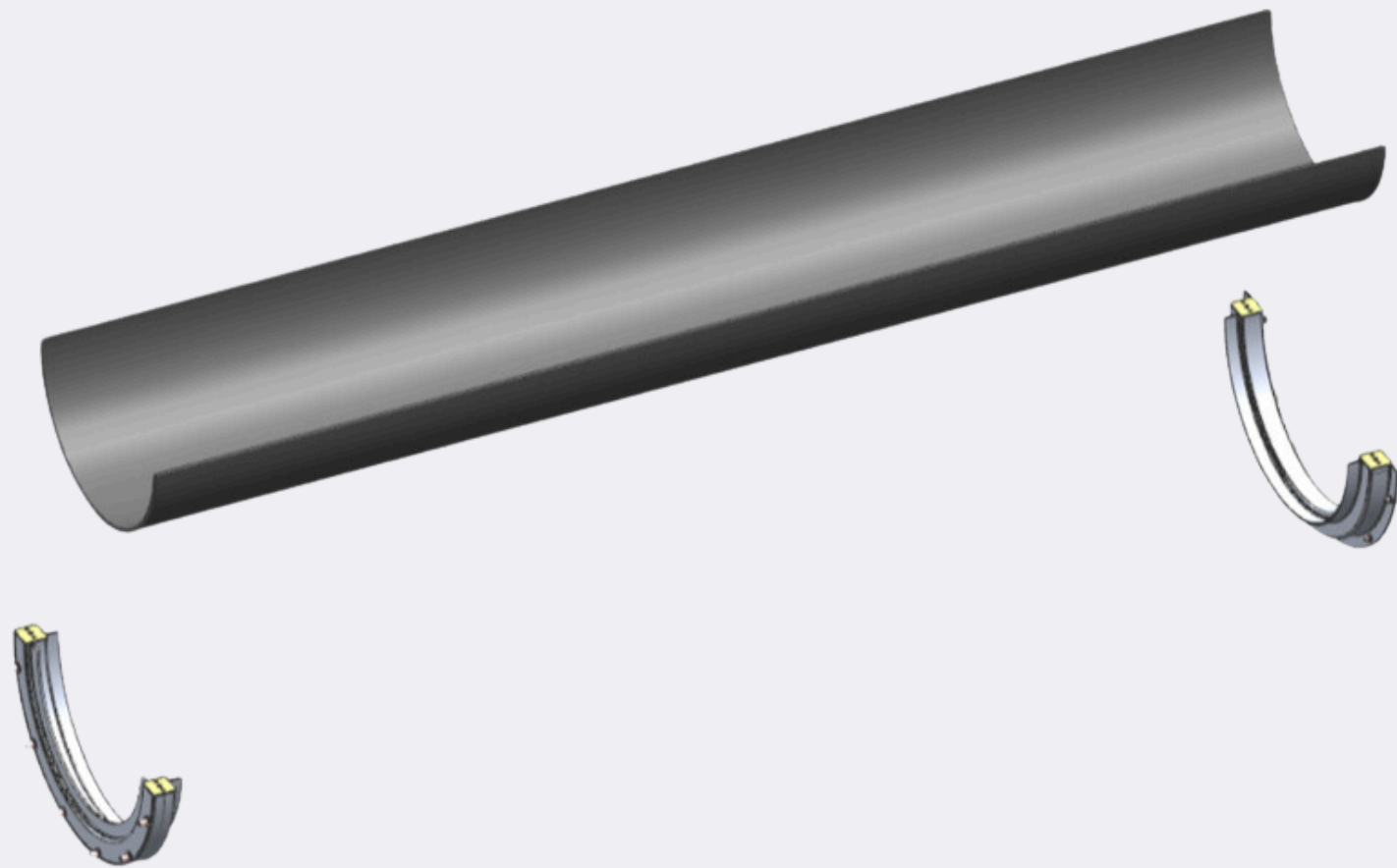
# Design

- Supports fit the cooling system



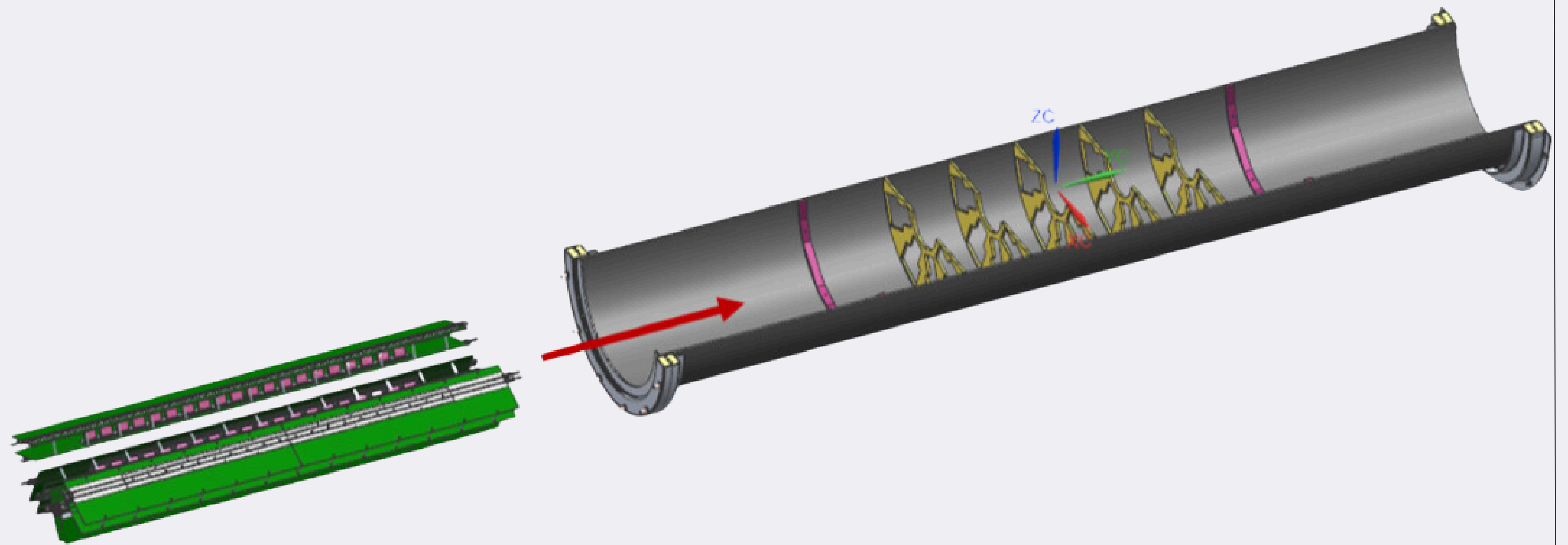
# Design

- Assembling



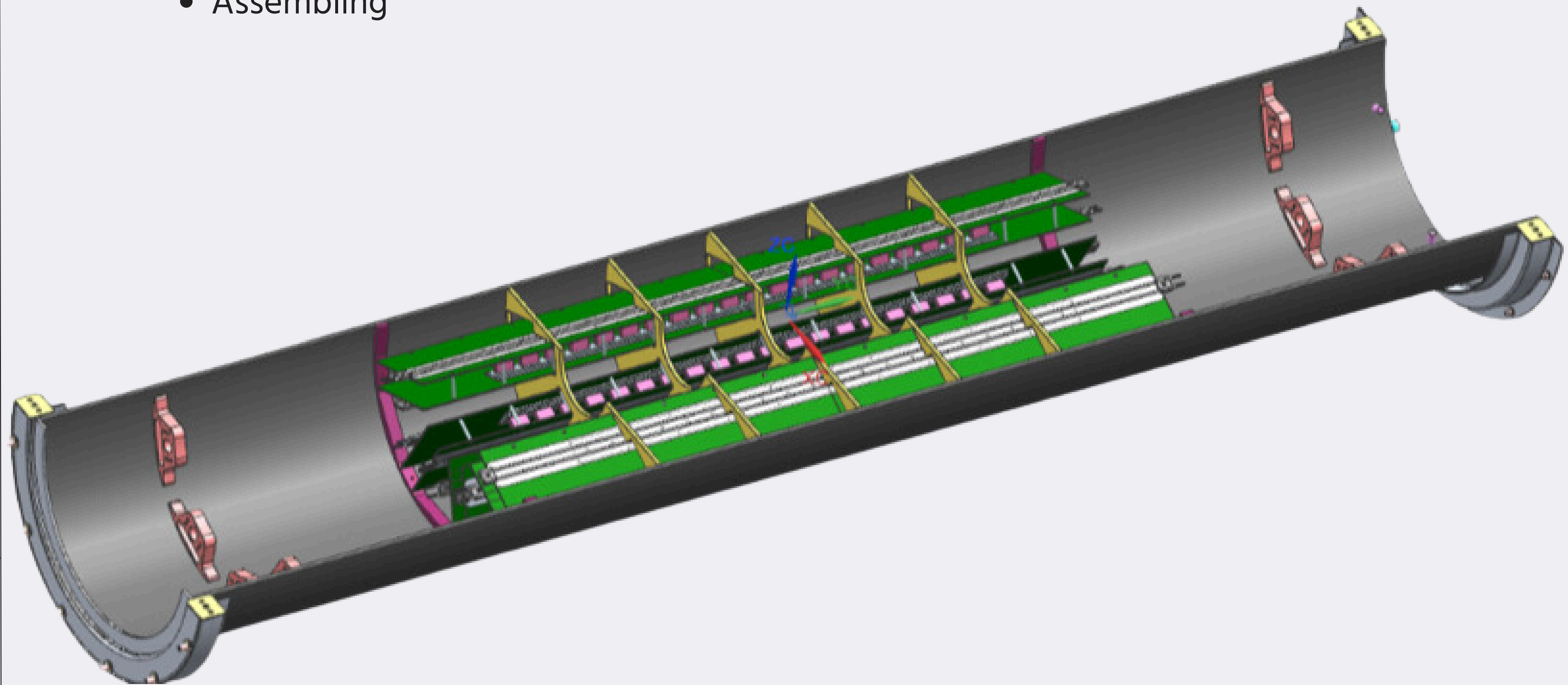
# Design

- Assembling



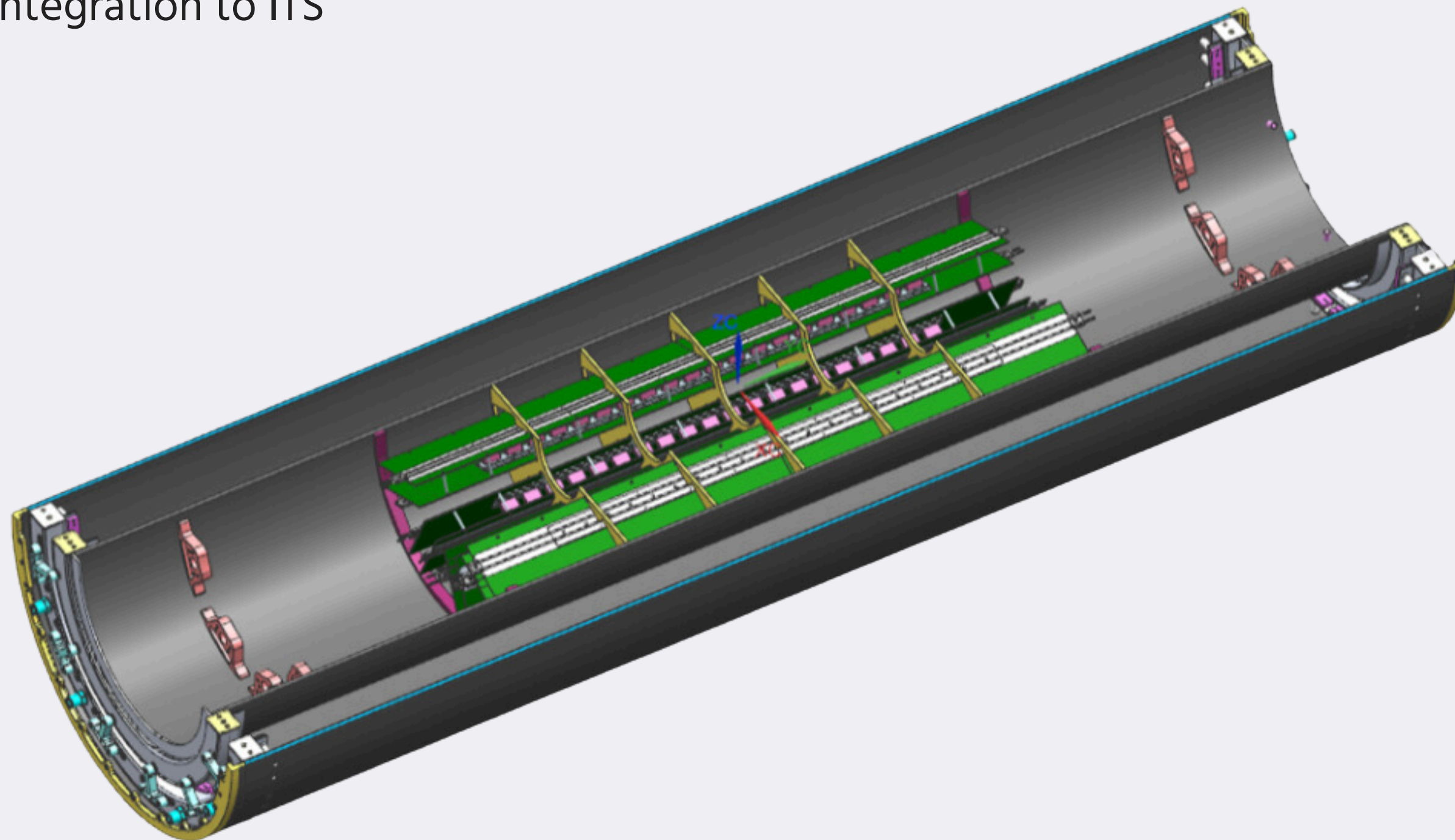
# Design

- Assembling



# Design

- Integration to ITS







03

# Simulations

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Efficiency of MiniBeBe as a trigger



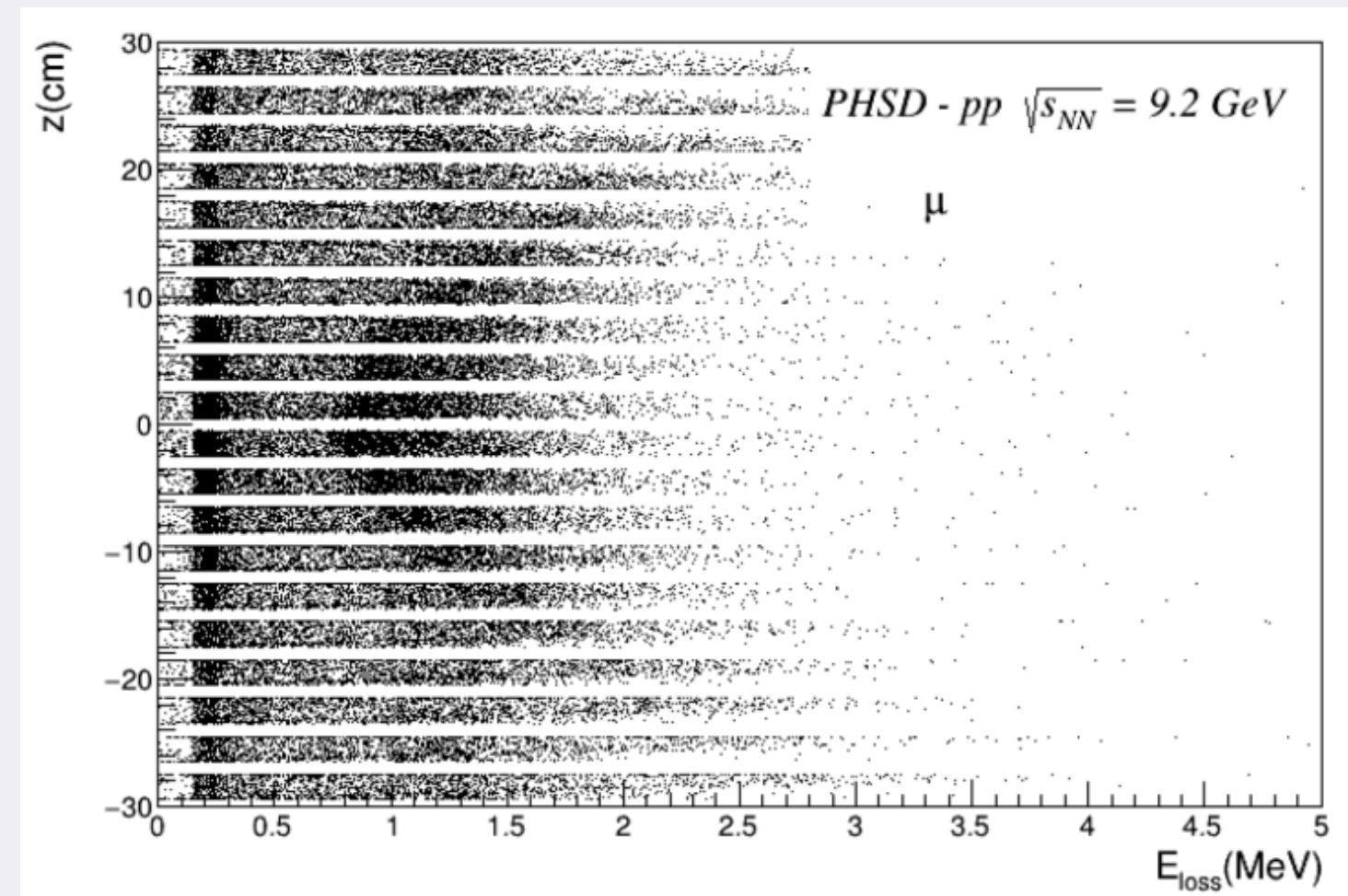
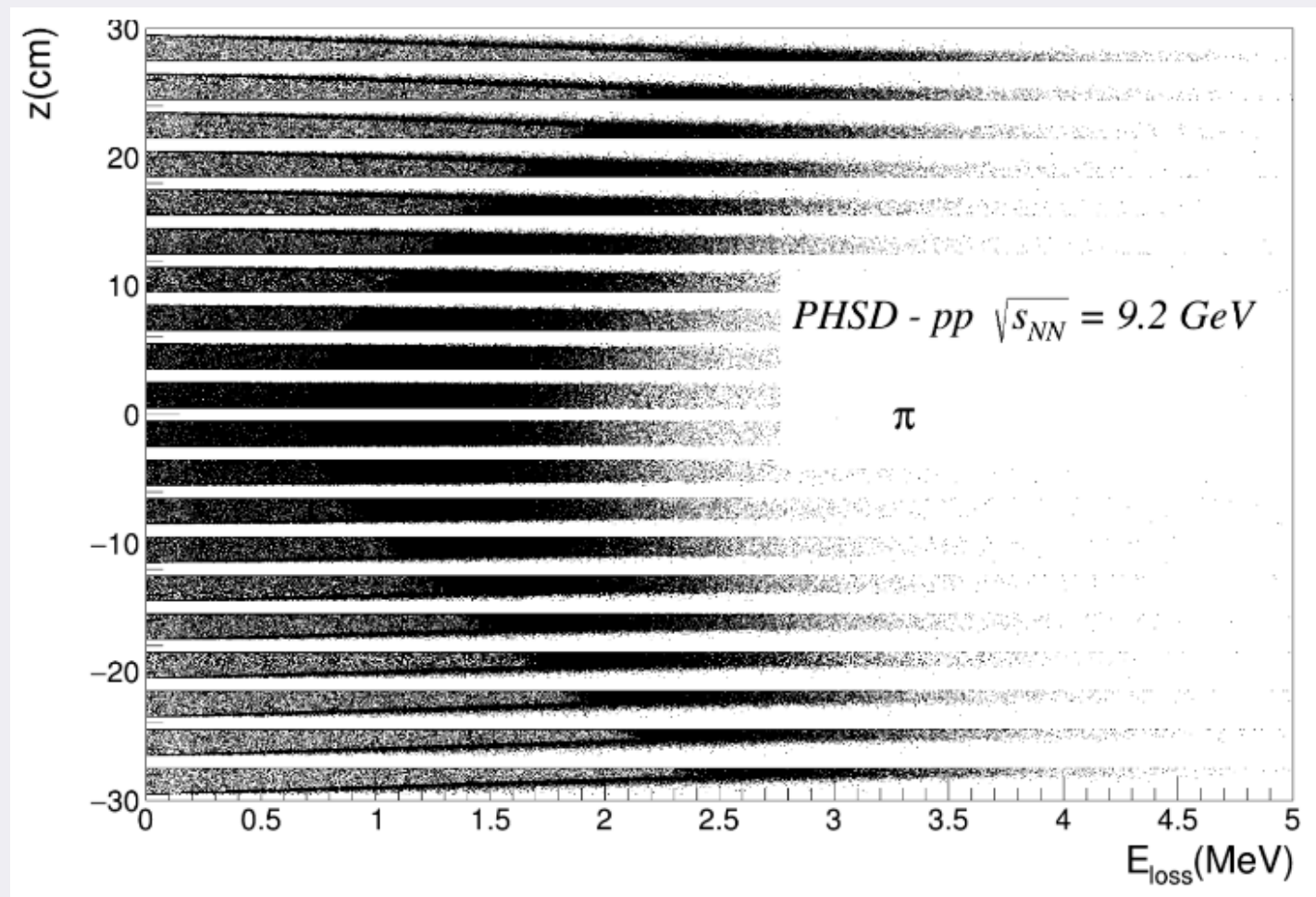


# Simulations

- MPDRoot
- 5M pp collisions @  $\sqrt{s} = 9.2\text{ GeV}$  with PHSD generator
- 1M BiBi collisions for comparison
- Smearing of primary vertex  $\sqrt{\sigma_z} = 50\text{ cm}$
- Maximal number of modules

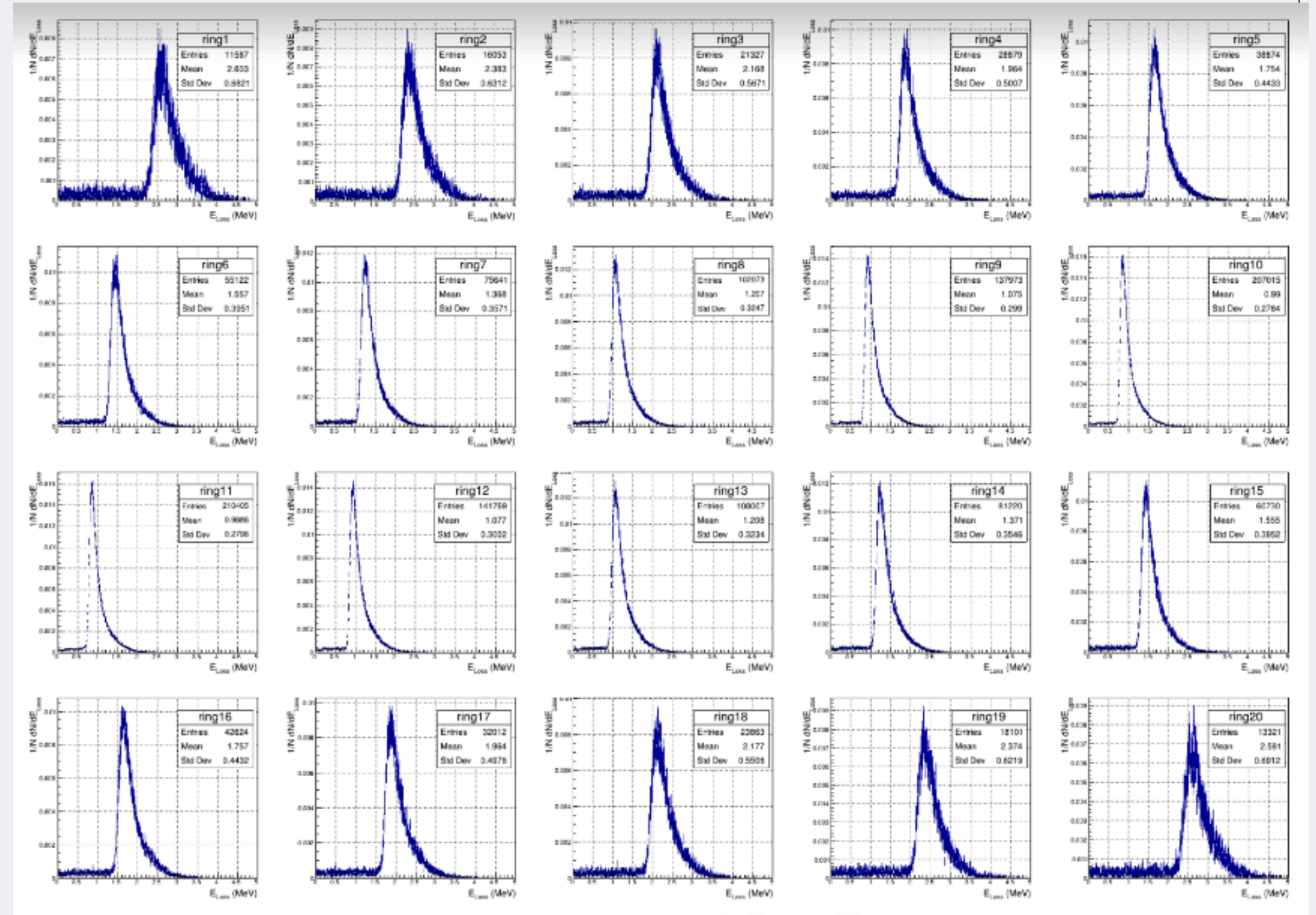
# Simulations

- Without smearing



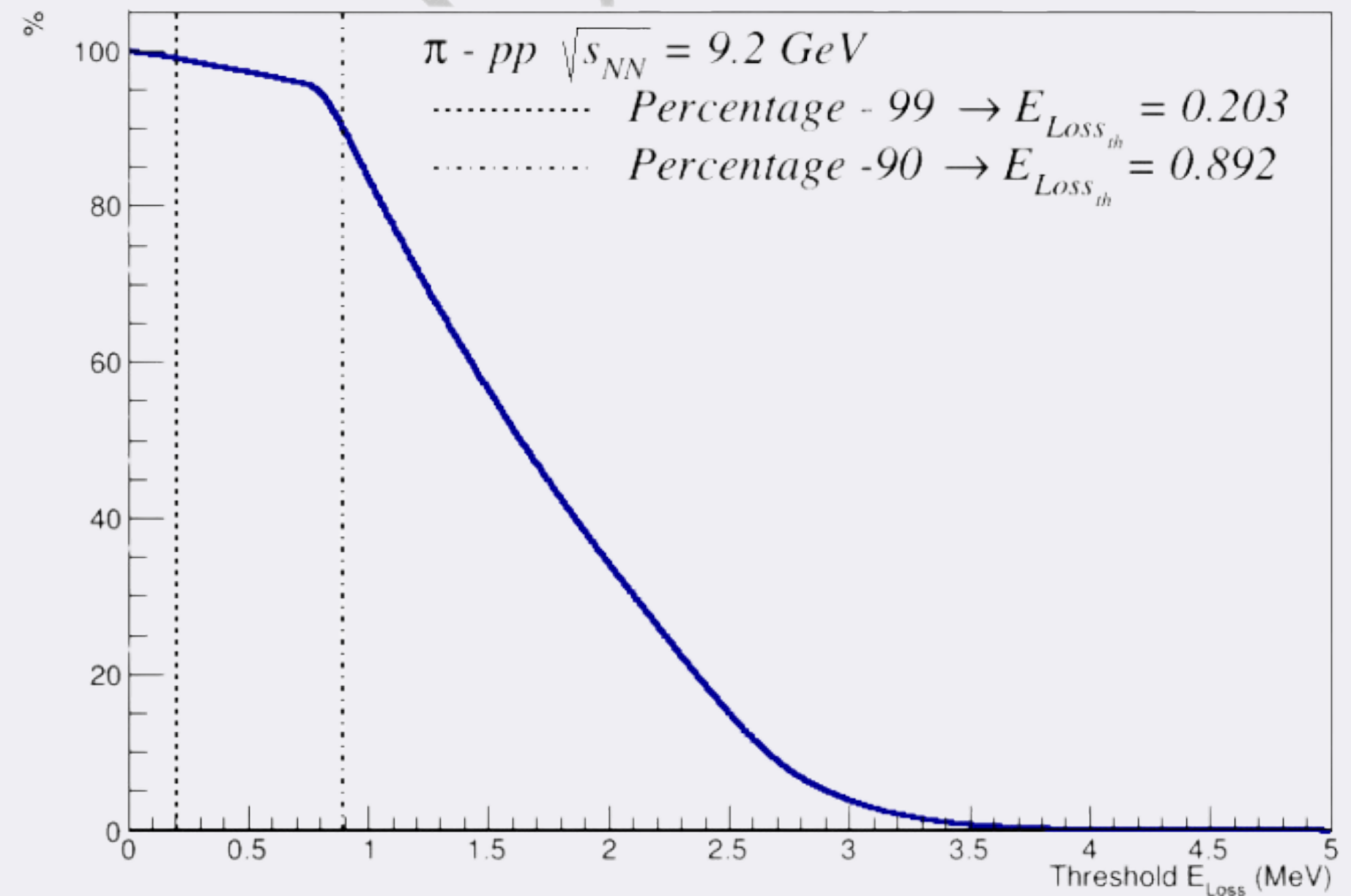
# Simulations

- Without smearing
- Energy deposition of pions at each ring.



# Simulations

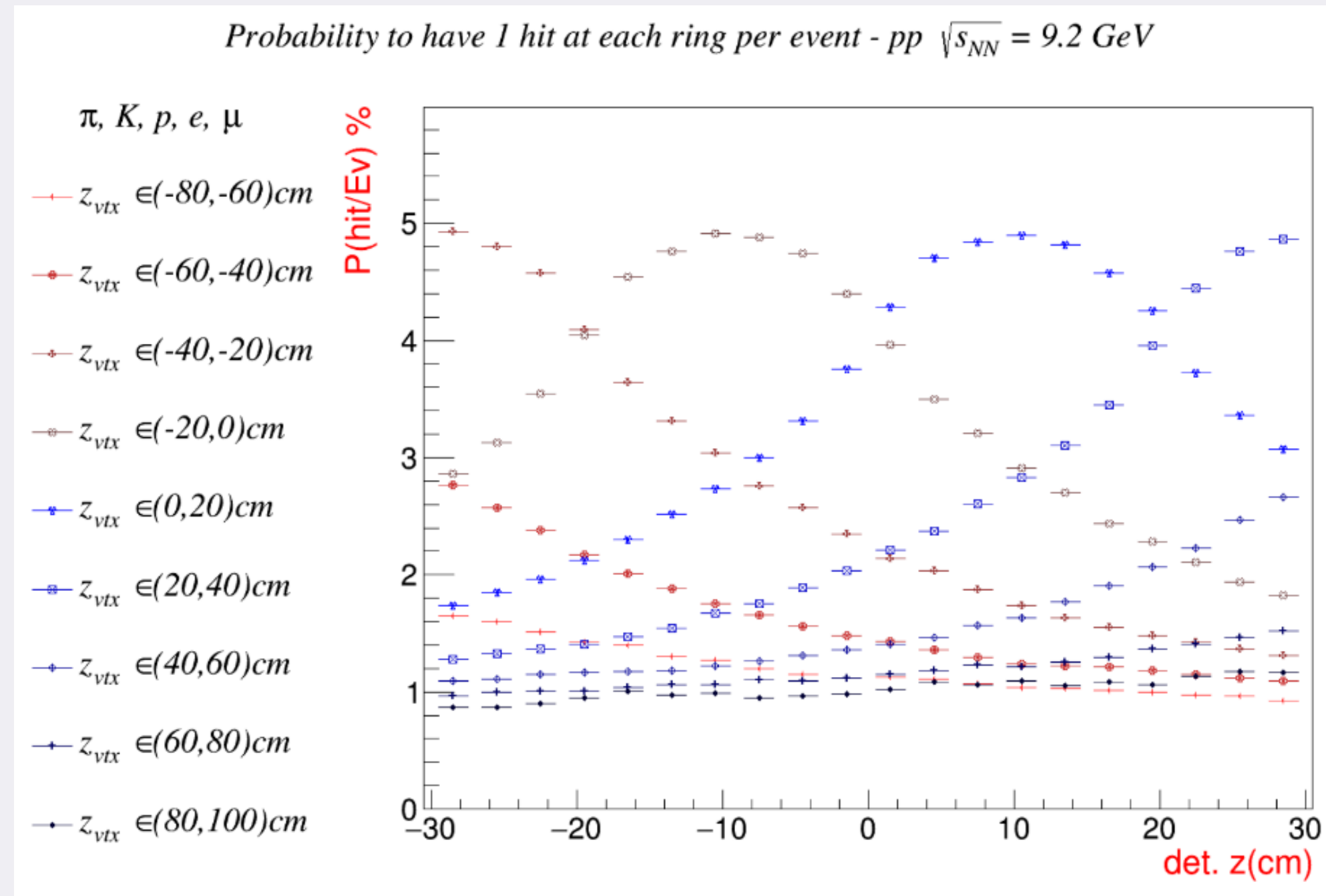
- Without smearing
- Threshold Energy to detect a pion with 99(90)% efficiency





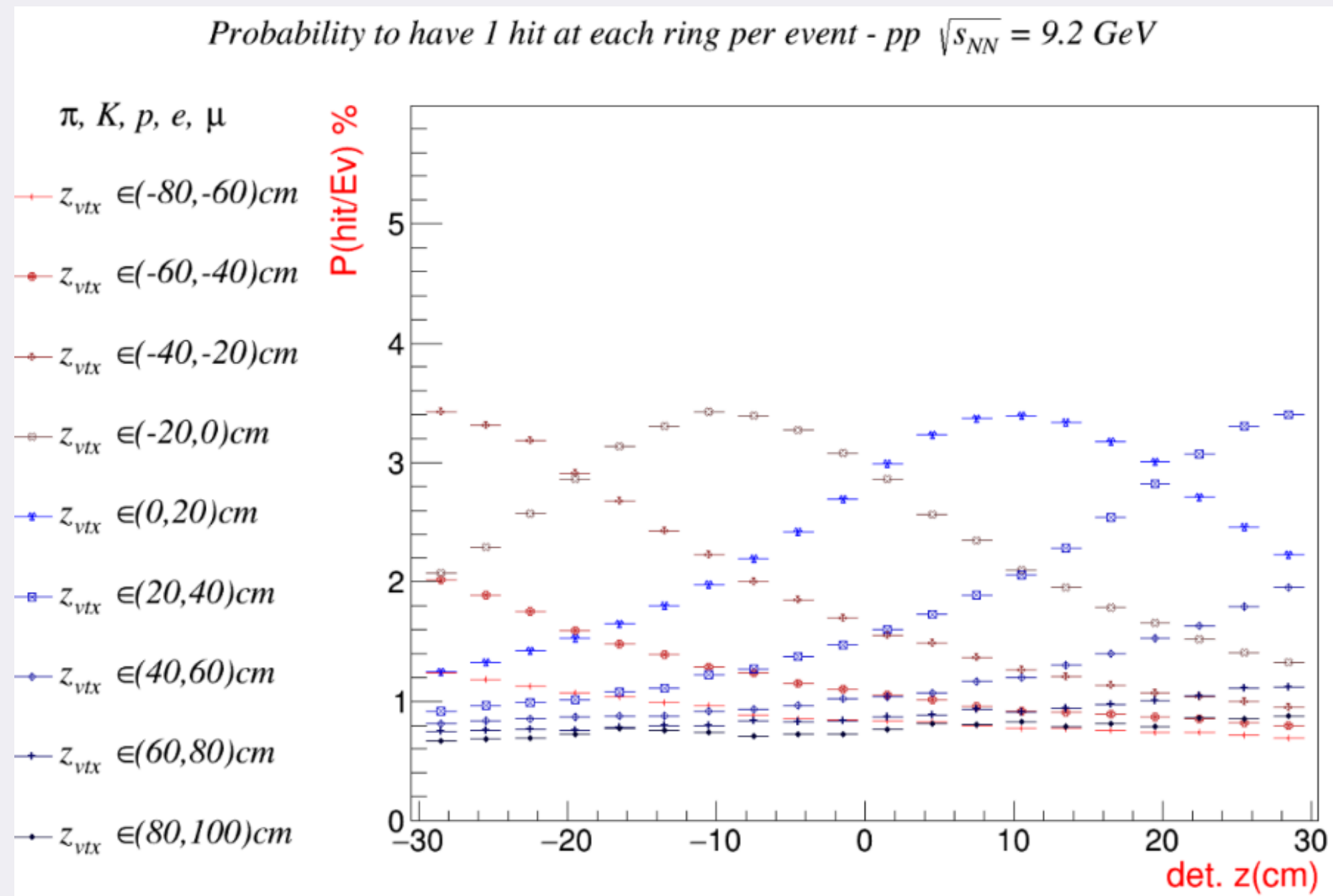
# Simulations

- Applying the cut of energy  $E_{th} > 2.03 MeV$



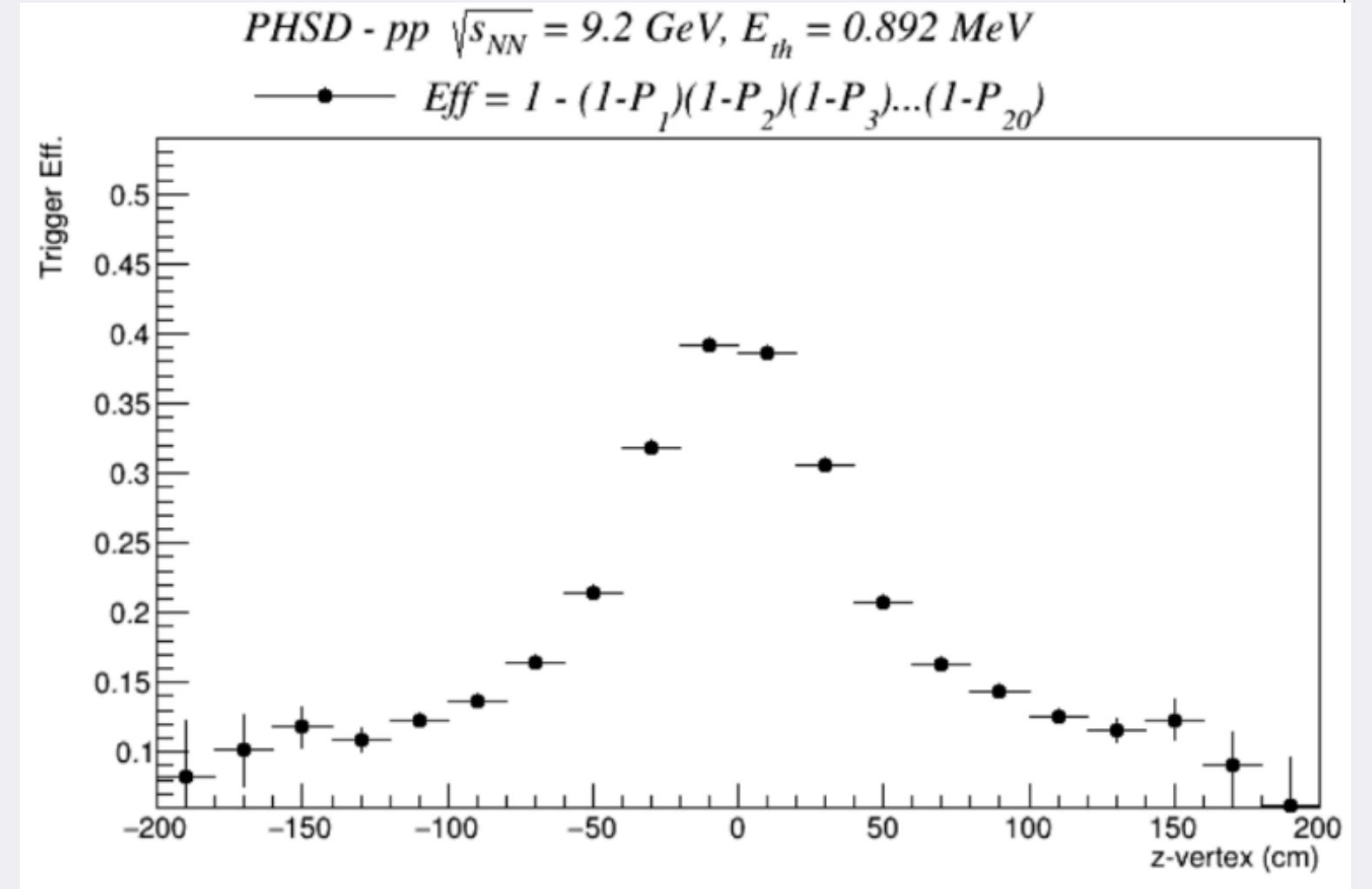
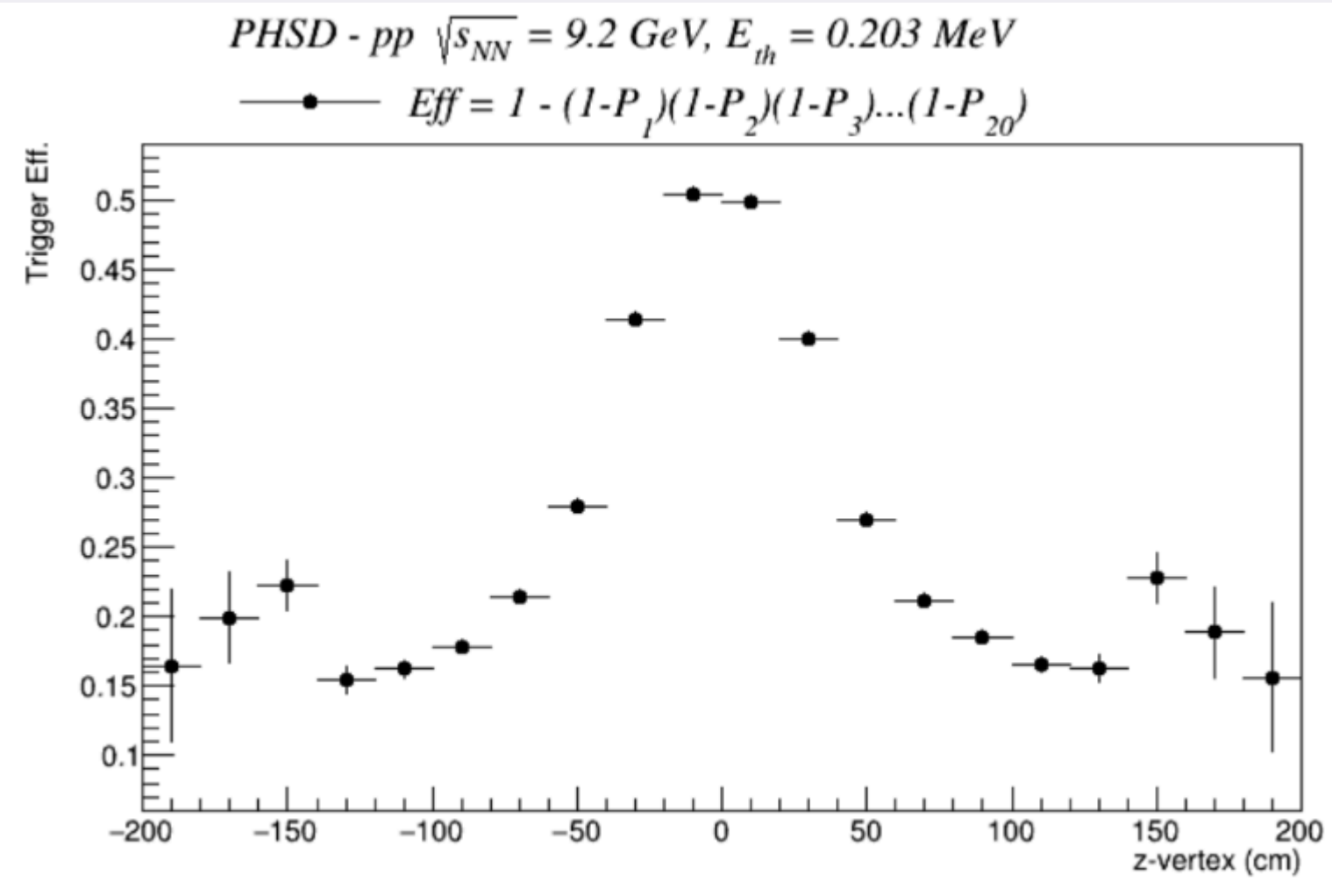
# Simulations

- Applying the cut of energy  $E_{th} > 0.892 MeV$



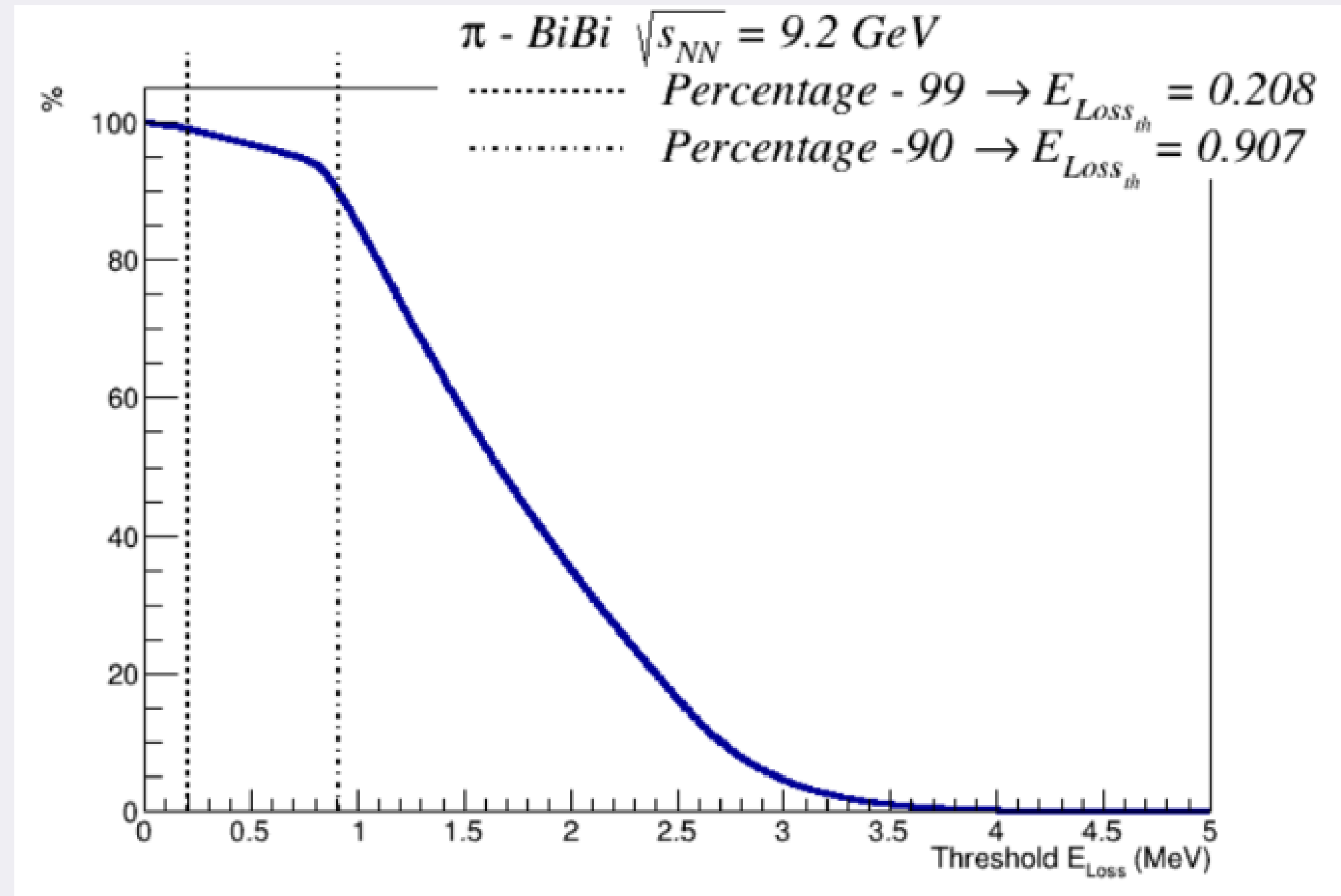
# Simulations

- Trigger Efficiency as function of the position of PV



# Simulations

- For Bi Bi collisions

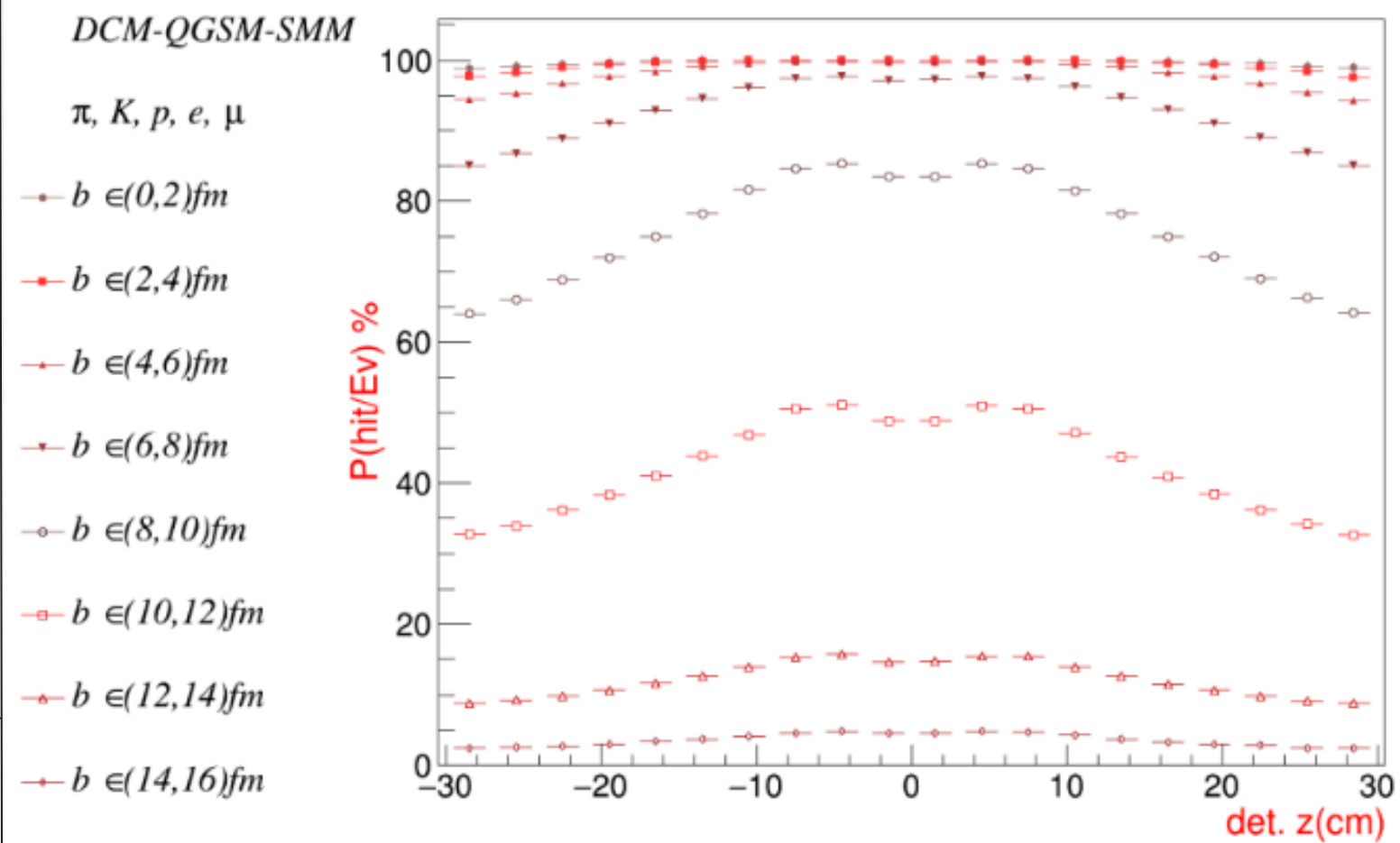




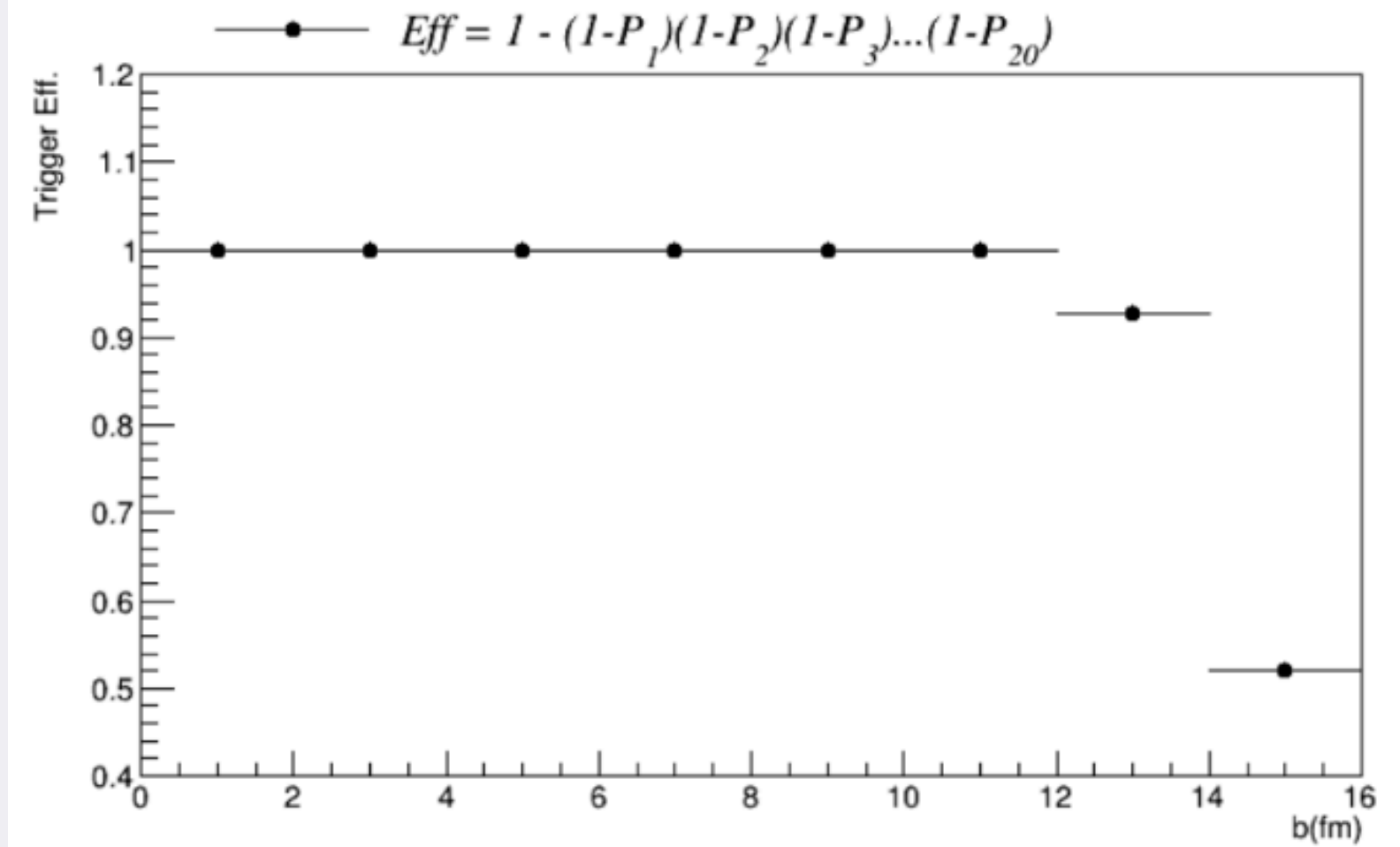
# Simulations

- For Bi Bi Collisions

Probability to have 1 hit at each ring per event - BiBi  $\sqrt{s_{NN}} = 9.2 \text{ GeV}$

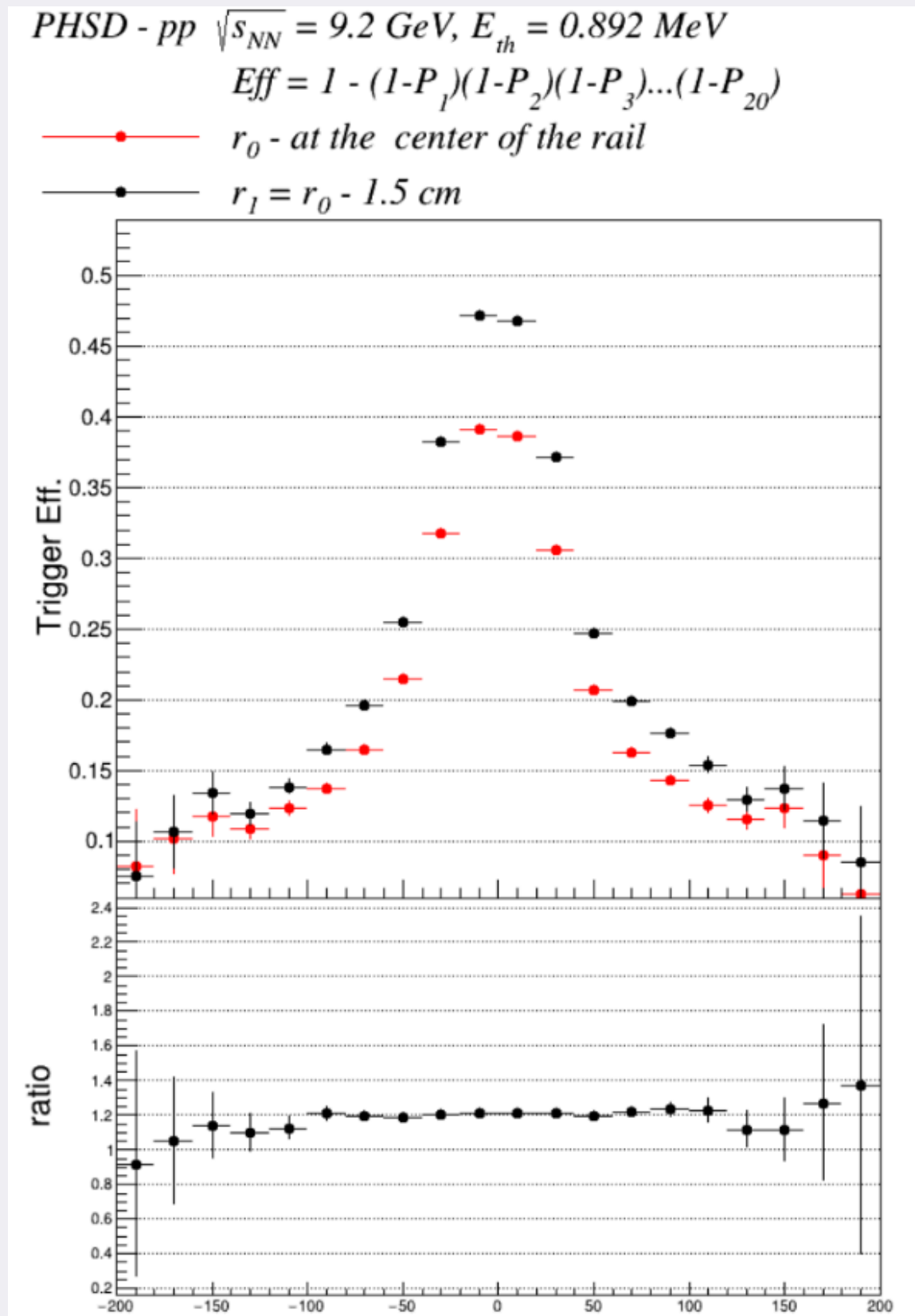
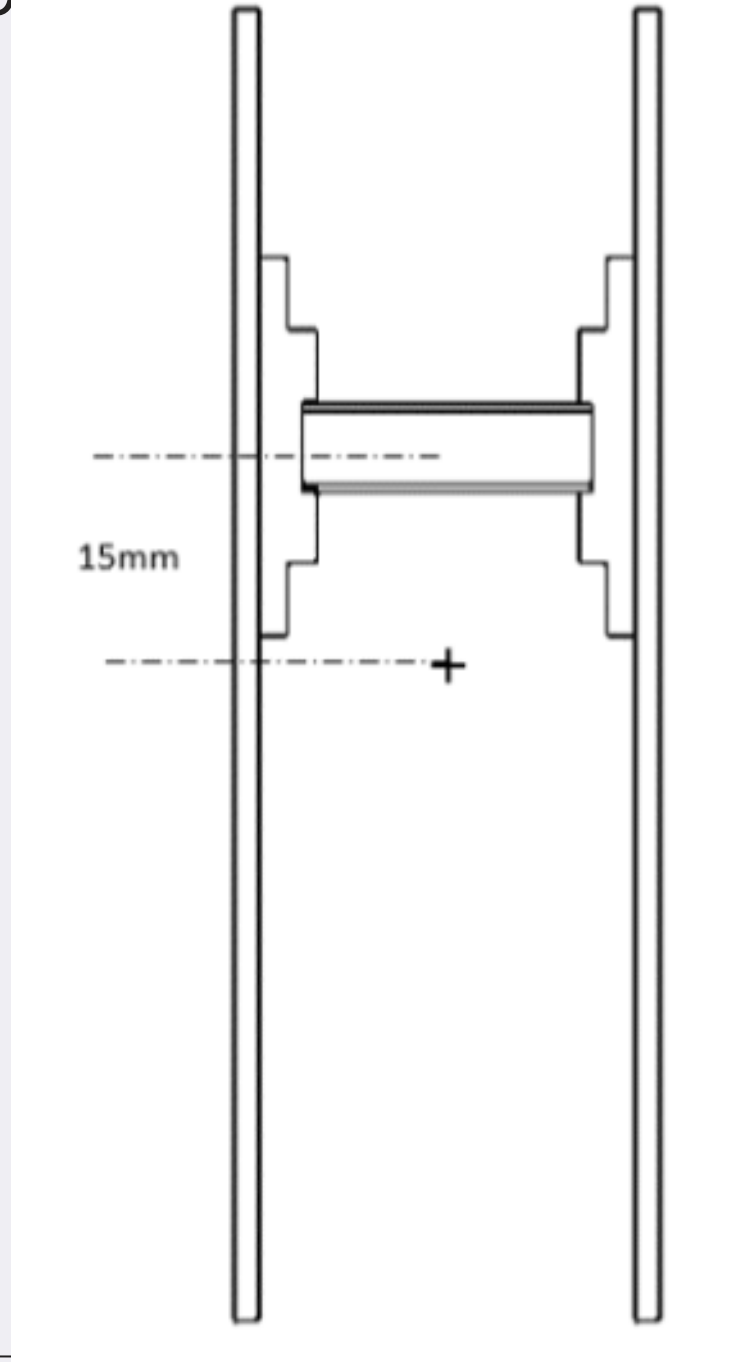


DCM\_QGSM-SMM - BiBi  $\sqrt{s_{NN}} = 9.2 \text{ GeV}, E_{th} = 0.907 \text{ MeV}$



# Simulations

- Moving the plastic scintillator





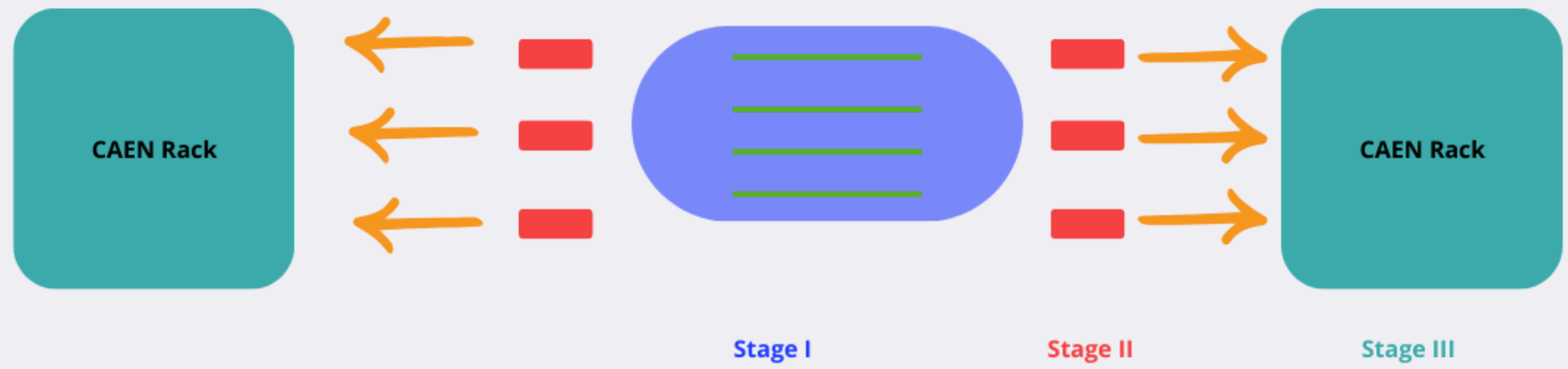
04

# Electronics

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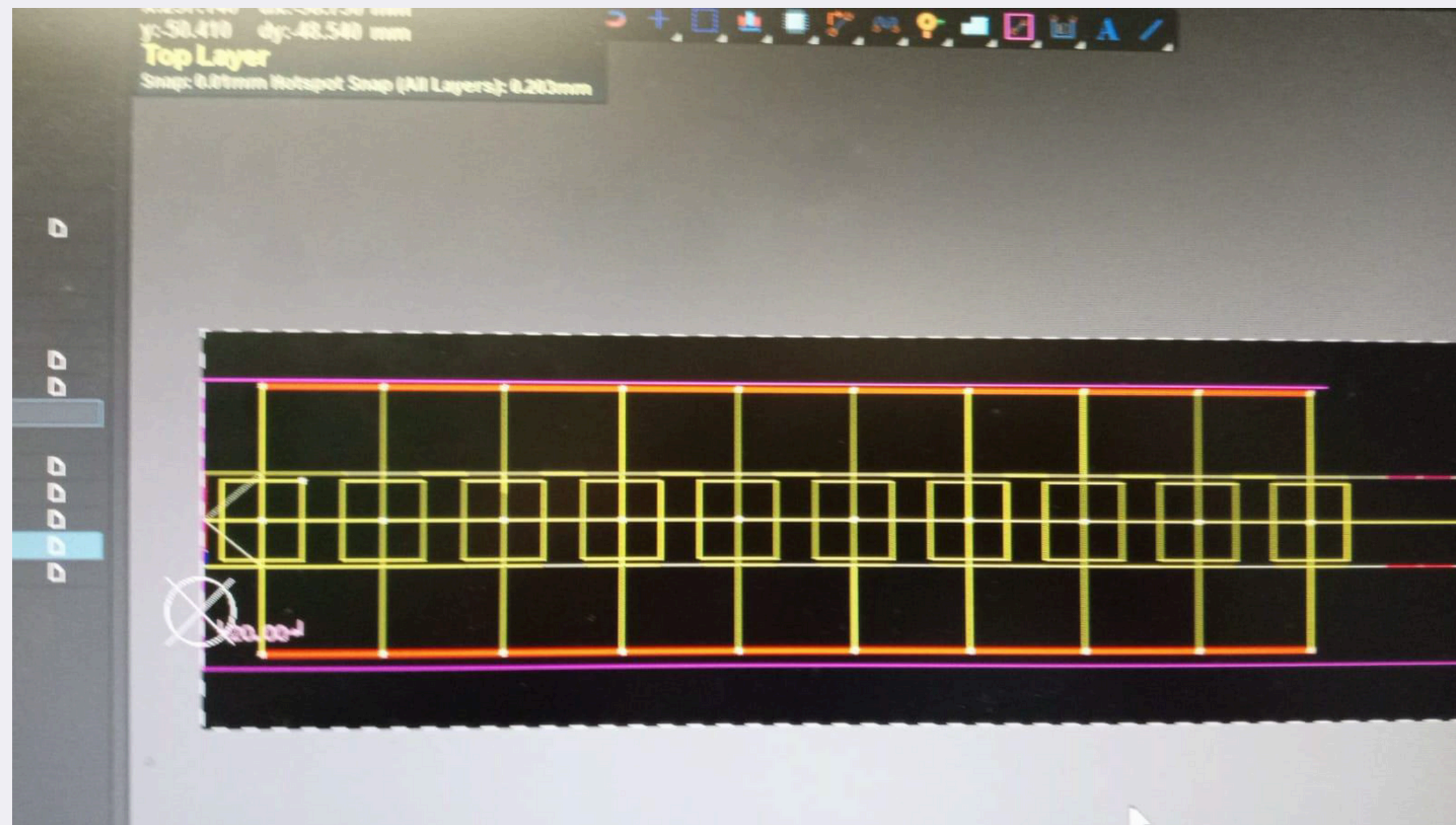
Design of Electronics of Mini BeBe





# Electronic Boards

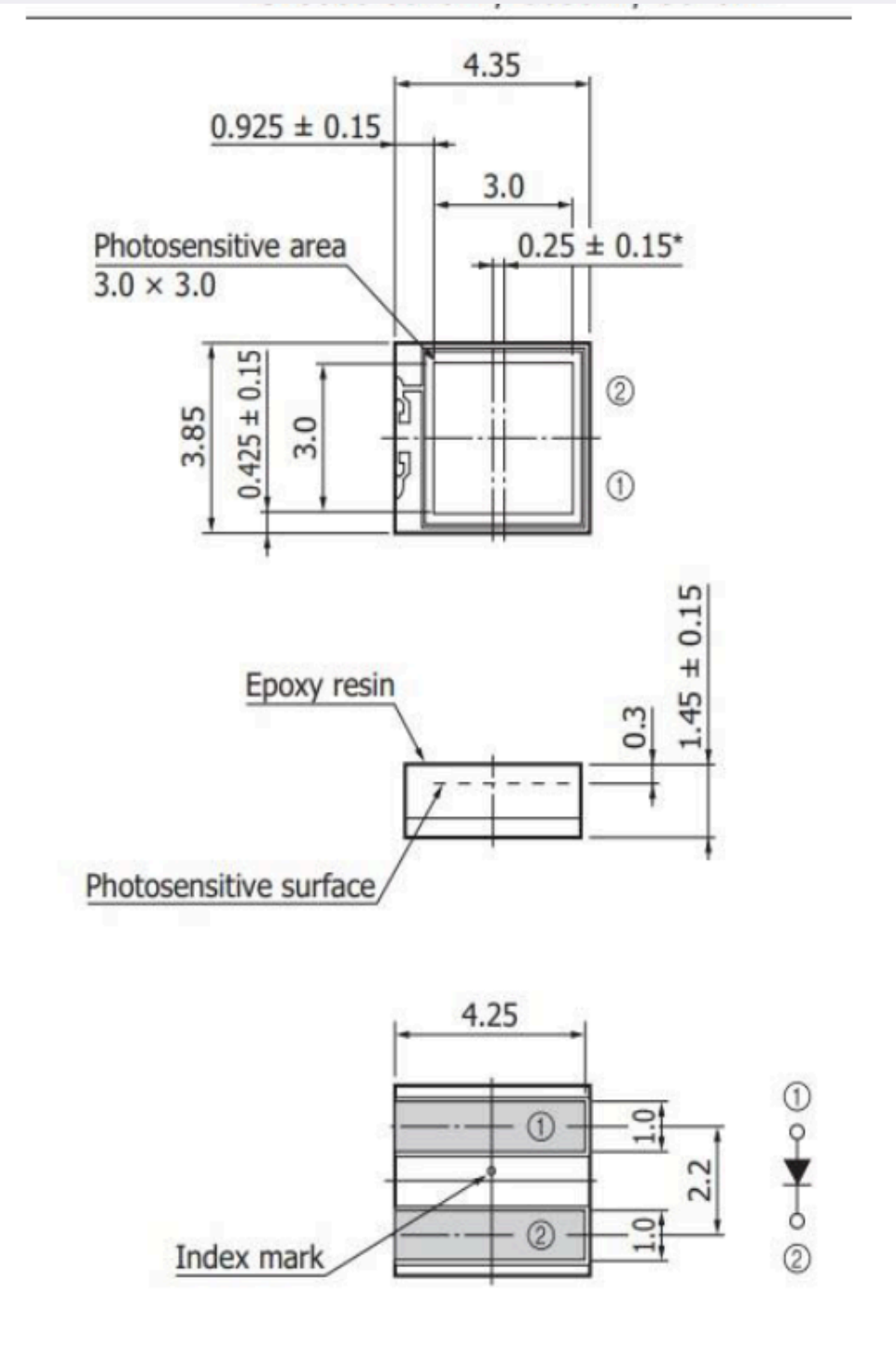
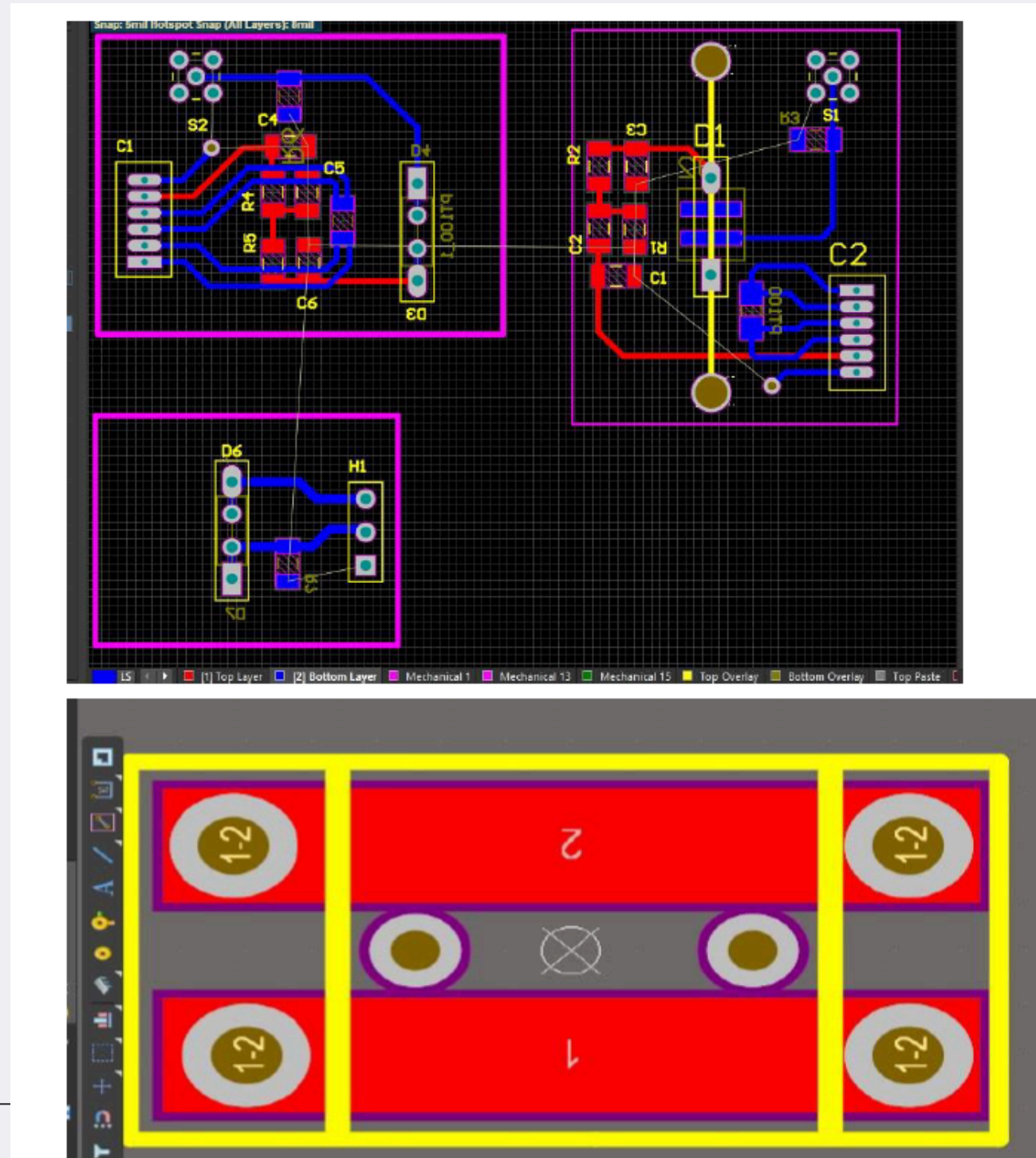
- Blueprints





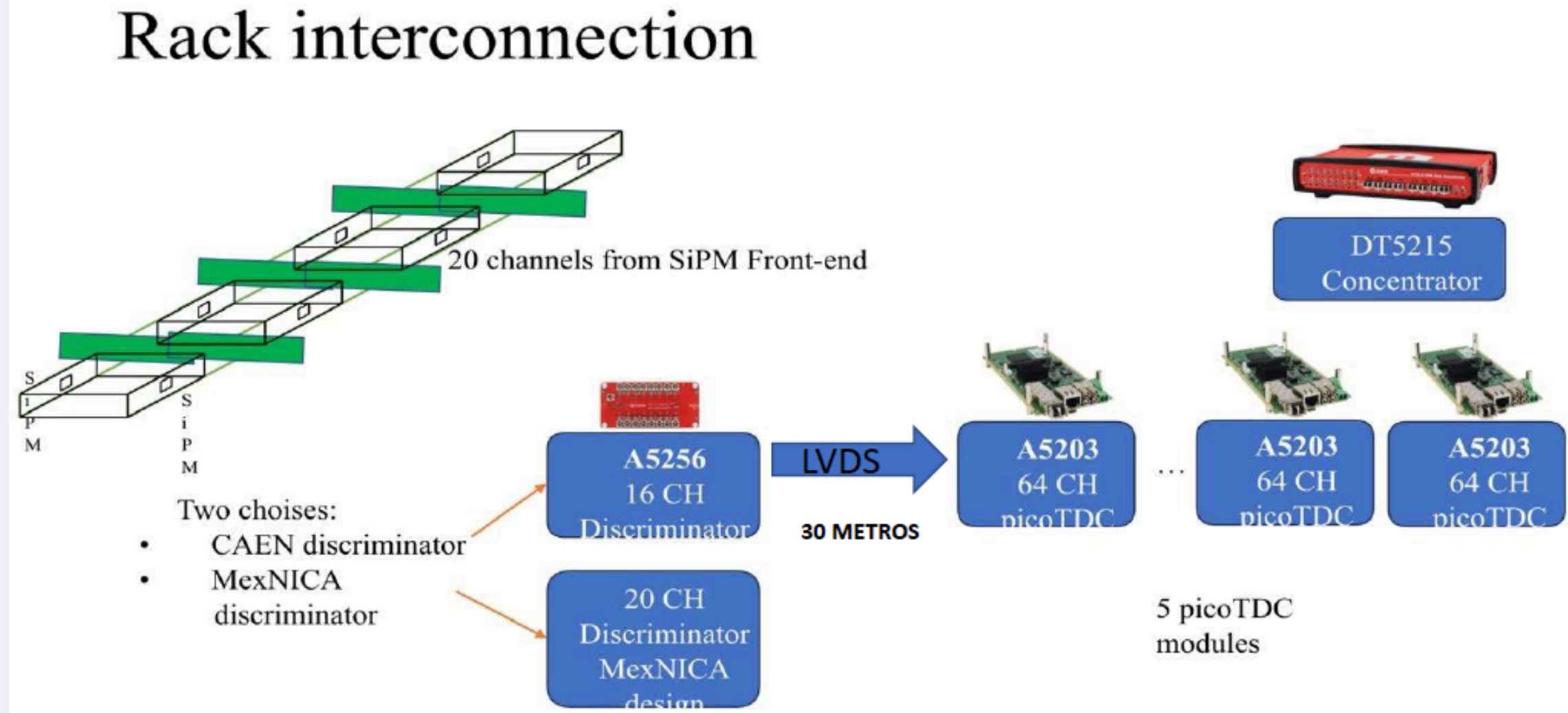
# Electronic Boards

- Blueprints



# Electronic Boards

- CAEN Modules
- Optic fiber connections
- PS per cell proper design
- Access for maintenance



OPCIONES  
-caen  
-FRONT END

<https://www.caen.it/products/a5255/>  
<https://www.caen.it/products/a5256/>  
<https://www.caen.it/products/dt5203/>



# Electronic Boards

- CAEN modules

**DT5203** ★ New  
Desktop 64 Channel picoTDC unit for FERS-5200

[Request a quote](#)

[Data Sheet](#) [Manual](#) [Downloads](#)

### Features

- 64-ch TDC unit for **high-resolution timing** applications housing the CERN picoTDC
- Part of **FERS-5200**, the CAEN platform for the readout of **large arrays of detectors** (SiPM, MA-PMTs, Gas Tubes, Si detectors, ...)
- Timing resolution: **LSB = 3.125 ps, RMS typ. ~ 7 ps**
- TDC dynamic range: **up to 26 bit (~ 210 μs). Extendable to 56 bit in the FPGA**
- Inputs: **differential LVDS signals** (max common mode = 1.2 V; max absolute voltage = 1.45 V). **NIM, TTL or analog signals through dedicated adapters**
- Acquisition of **leading/trailing edge Time of Arrival (ToA)**, or **leading edge ToA plus Time over Threshold (ToT)** of the input signals
- Scalability and easy-synch**: up to 128 cards (**8192 channels**) can be managed

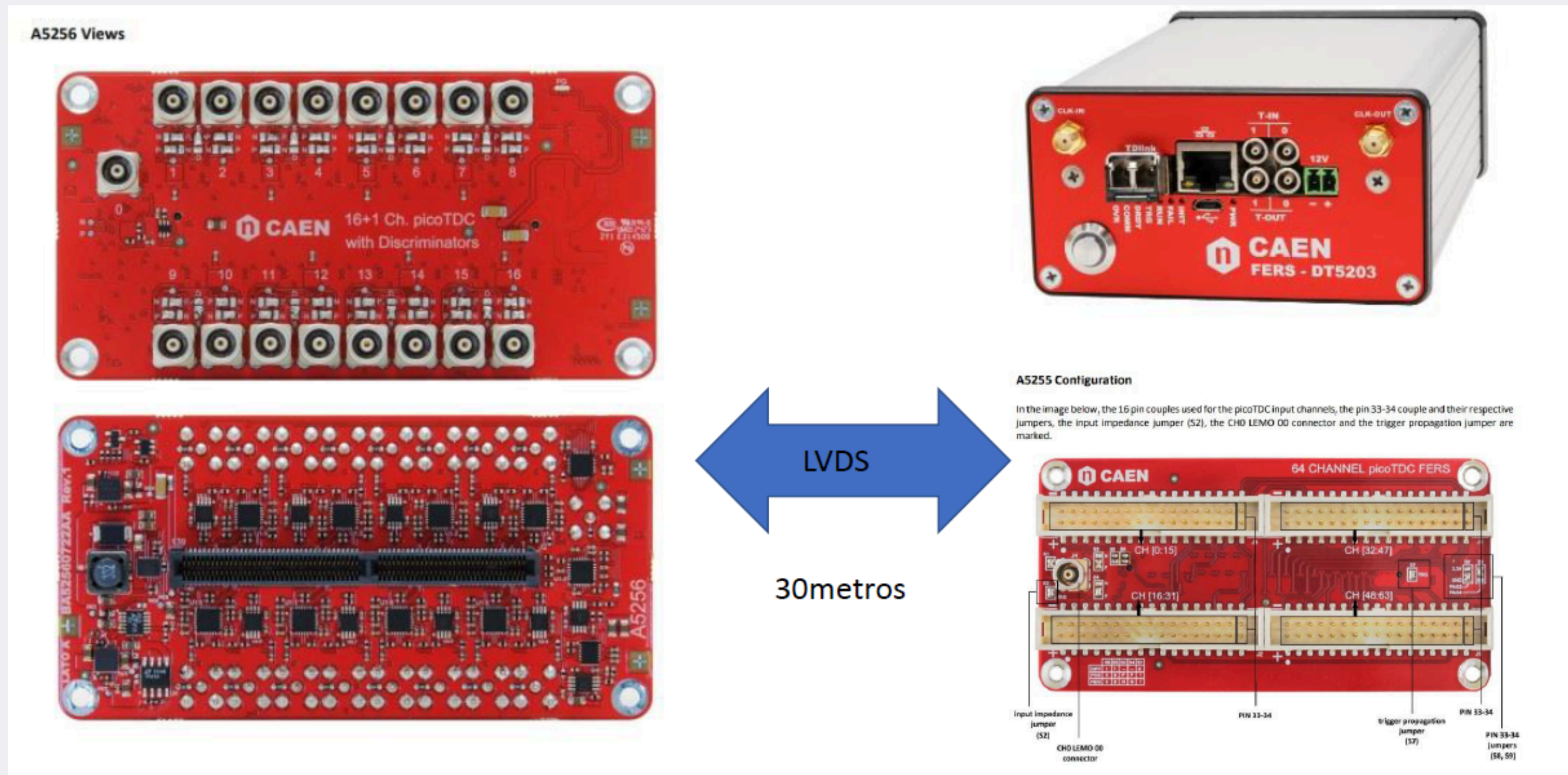
More info

**Fig. 9.1:** Simplified block diagram of the A5203(B)/DT5203 FERS-5200 unit. The expansion mezzanine is embedded only in the A5203B board type.



# Electronic Boards

- CAEN Modules





# Electronic Boards

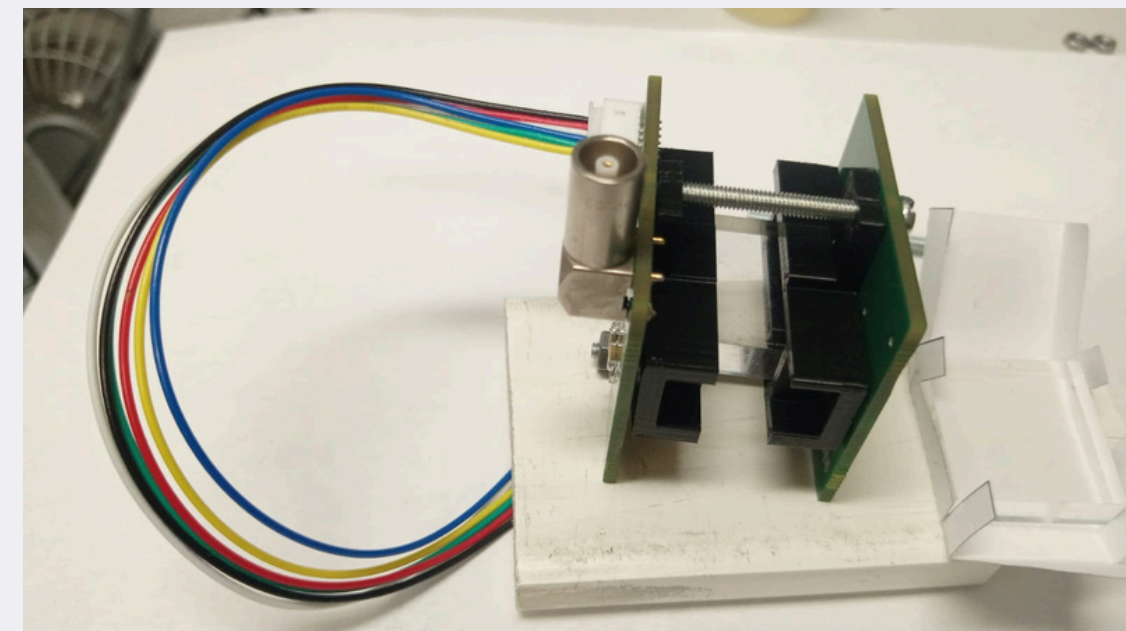
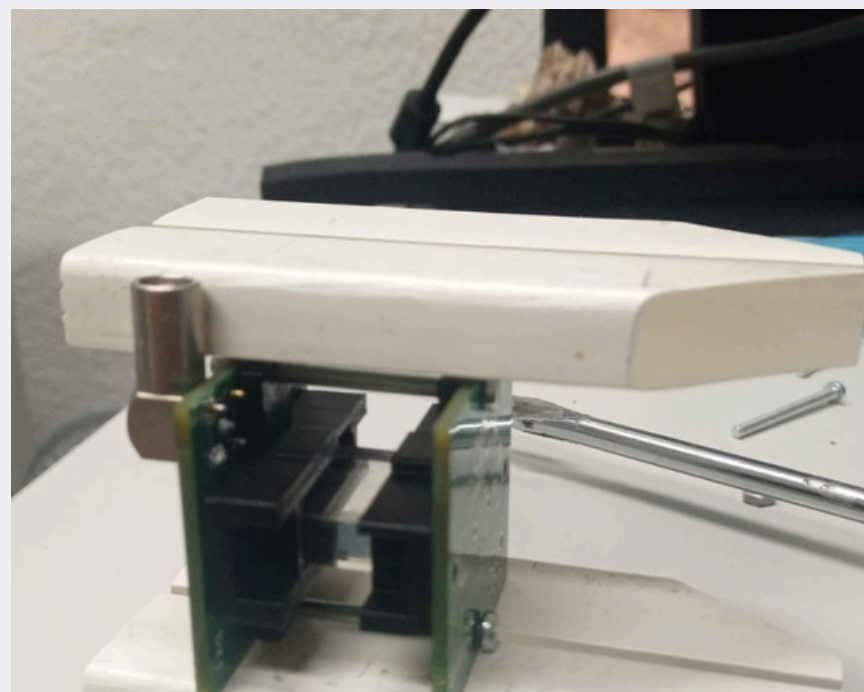
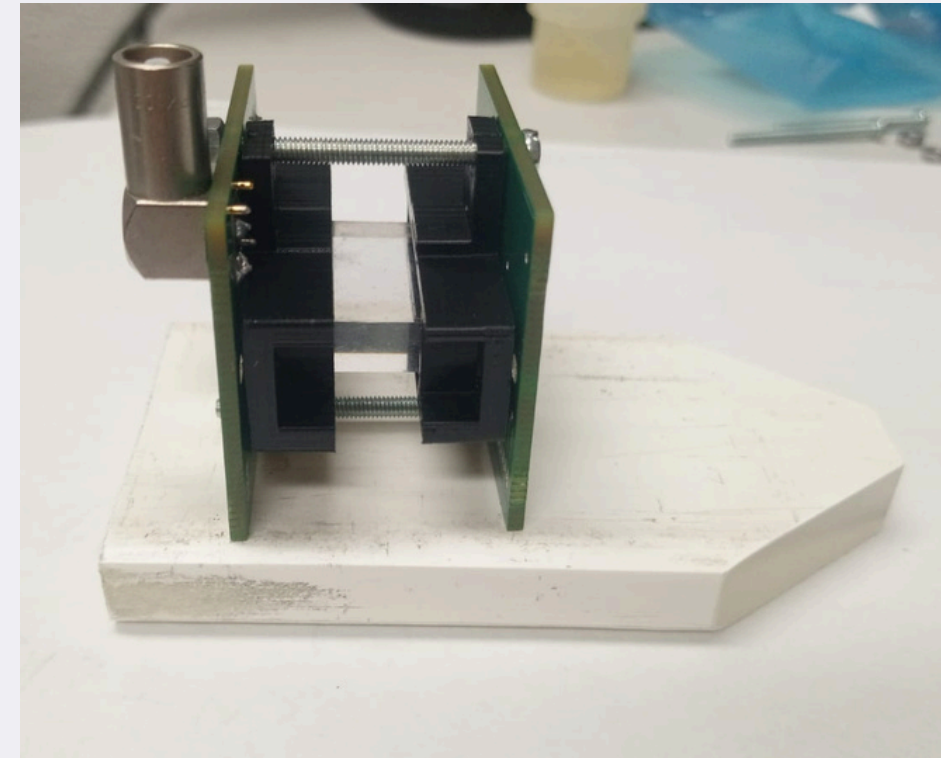
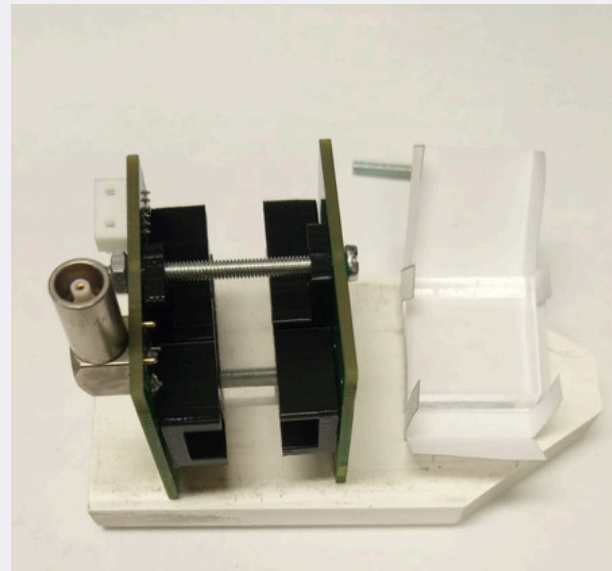
- Cables and connectors





# Electronic Boards

- H-Cells





- 4-5 Months for electronic design
- Test and adjustments
- 1 year to complete the project
- Collaboration approval
- Construction and Instalation *in situ*
- Ready for phase 0

Thanks!  
¡Gracias!

