PIERRE AUGER OBSERVATORY

AugerPrime SDEU ORR

Overview

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for the SDEU team

Malargüe, 14 April 2024

Introduction

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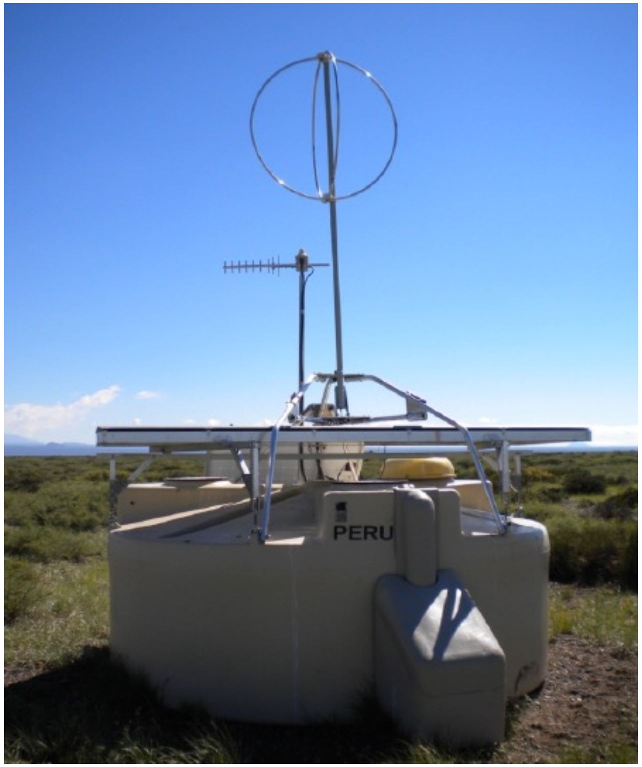
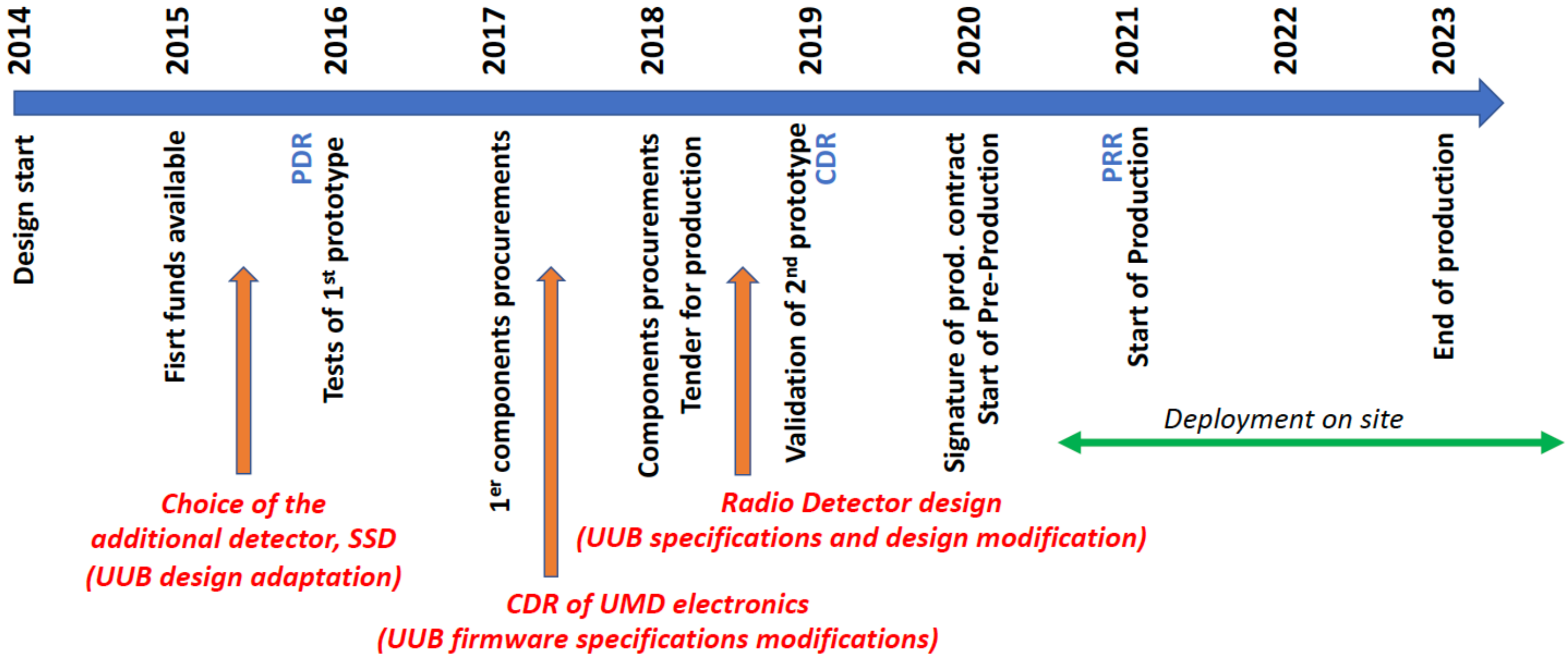


The Surface Detector Electronics Upgrade (SDEU)

- Reads and processes signals from WCD PMTs, SPMT, and SSD PMT
- Provides interface to RD and UMD (RD: Trigger, COMMS and power, UMD: Trigger)
- Improves the dynamic range (SPMT), resolutions, and data processing capabilities
- Firmware/software adapted from the previous one
- Local triggers adapted from previous ones (compatibility triggers at 40 MHz)
- Electronics gathered on a single board (UUB)
- Uses existing communication system (main array, infill array: UMD COMMS)
- Uses existing power system except for new solar panels to accommodate increased power consumption due to RD
- Uses existing mechanical interfaces and enclosures

Timeline

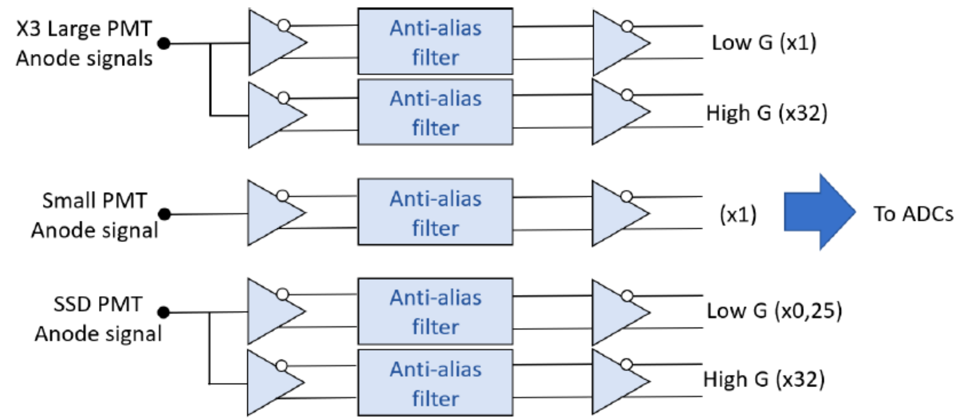


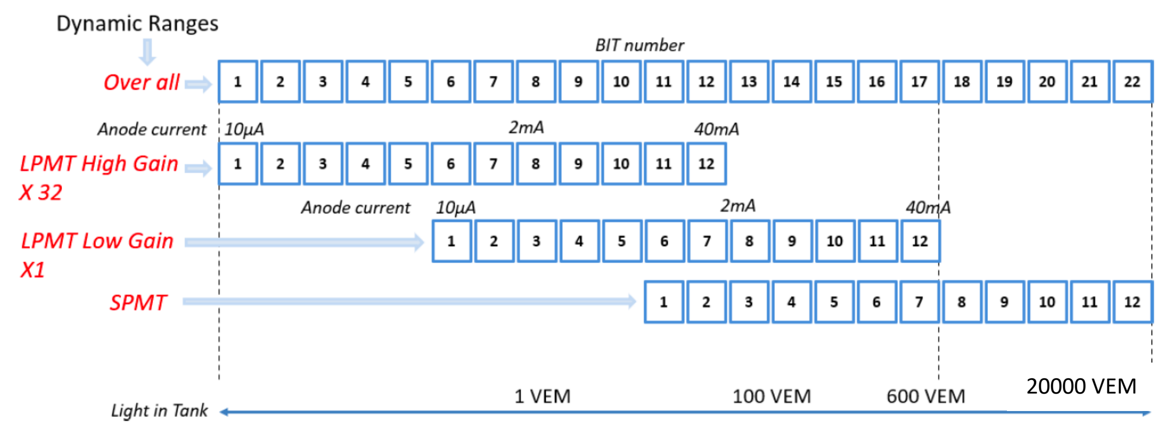
- 2016: Engineering Array to validate the design and to test the integration into Observatory operation
- End of 2020 – July 2023: Deployment of SDEU (UUB together with SPMT)
- End of 2020 – today: Commissioning

Design characteristics: Front-end

Increased WCD dynamic range by adding 1’’ PMT (SPMT, Hamamatsu R8619) to the three 9” PMTs (Photonis XP1805) of the WCD.

- 10 ADC analog inputs to handle the two gains for each of the three existing PMTs, the added PMT of the SSD, and the SPMT (plus a spare channel).
- Differential signal amplification with two amplifier stages
- A 7th-order Bessel low-pass filter with 60 MHz cutoff frequency
- Commercial 12-bit 120 MHz dual-channel FADCs (Analog Devices AD9628)



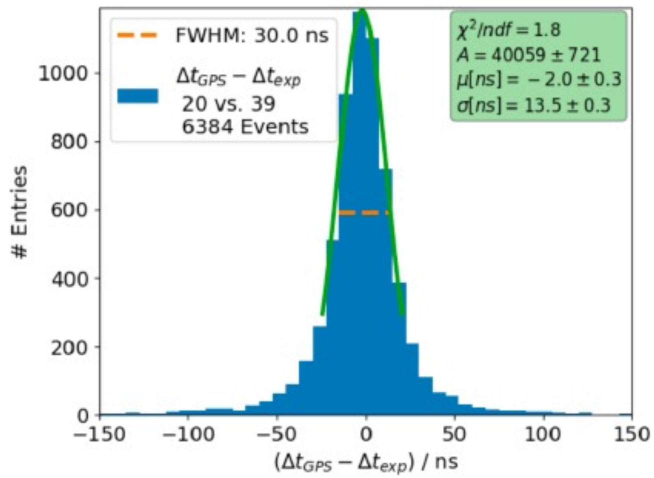


The intrinsic electronic noise measured in laboratory on the high-gain channels is about 2 LSB and 1/2 LSB on the low-gain channels. Cross-calibration measured in laboratory is 32.2 ± 0.3 for the WCD channels and 126.7 ± 1.3 for the SSD channels.

Design characteristics: Timing

- Synchronization by tracking variations of the local 120 MHz clock with respect to the 1 PPS signal of the Global Positioning System (GPS)
- Synergy SSR-6TF timing GPS receivers, functionally compatible with the Motorola Oncore UT+ GPS used with previous electronics
- Architecture of the time-tagging firmware module parallels the design concept used in the former electronics
- GPS receivers verified in laboratory before shipping to the Observatory

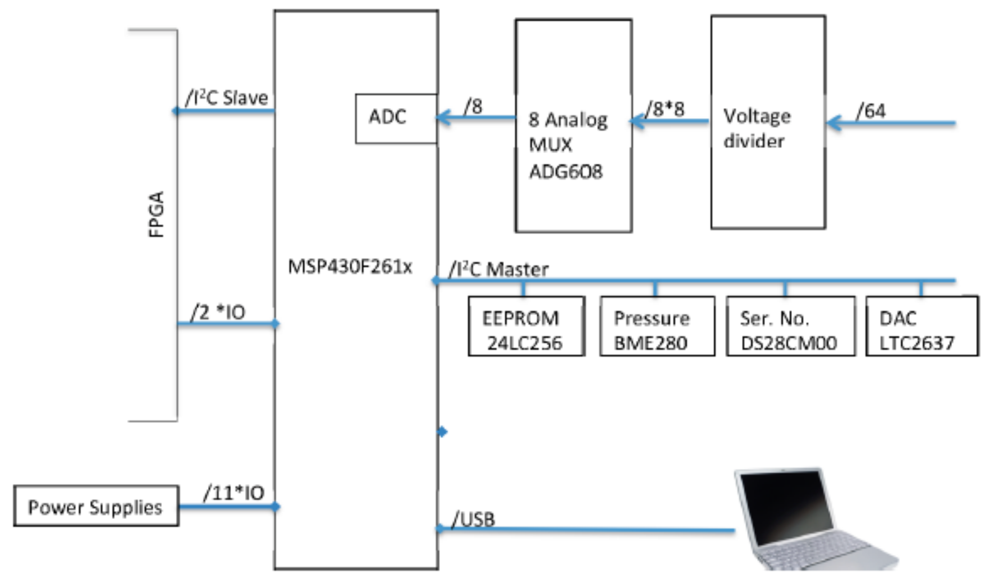
The relative timing accuracy (variance on timing of common signal between two SSR-6TF receivers) was measured in laboratory to be around 2ns and in the field between two detector stations (with fiber) around 5ns.



Measured timing resolution on showers using 2 nearby stations. Single station resolution is 13.5/√2 = 9.5 ns.
The relative timing accuracy between two SSR-6TF receivers is about 2 ns.

Design characteristics: Control and monitoring

- 16-bit RISC CPU ultra-low-power micro-controller (MSP430)
- Controls and monitors the PMT high voltages and various supply voltages
- Provides watchdog and reset functionality
- Controls 16 logic I/O lines, steers a 12-bit DAC with eight analog outputs, and senses through multiplexers up to 64 analog signals with its internal 12-bit ADC

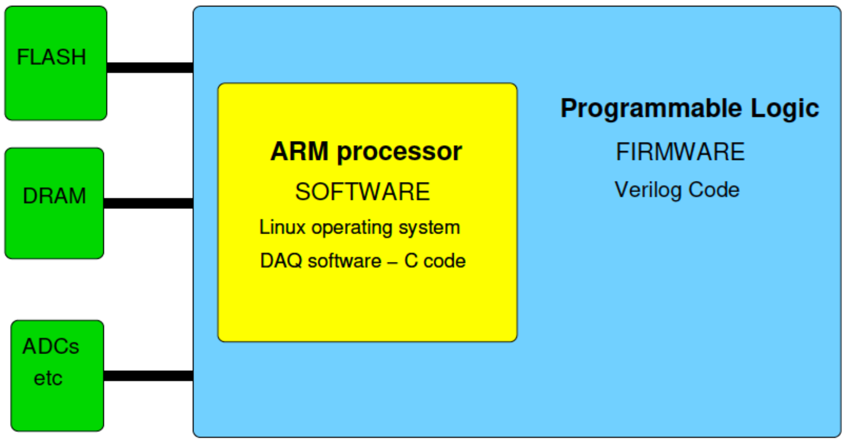


Monitoring works, need to update quality cuts and alarms.

Design characteristics: Firmware/Software

- The UUB architecture designed with a Xilinx Zynq FPGA containing two embedded ARM Cortex A9 333 MHz microprocessors
- The FPGA connected to a 4-Gbit LP-DDR2 memory and a 2-Gbit Flash memory
- The FPGA implements all basic digital functions such as the read-out of the ADCs, the generation of triggers, the interface to LED flasher, GPS receiver, clock generator, and memories
- High-level functions like data handling and communications with the radio transceiver are implemented under Linux.

Xilinx Zynq FPGA



Multi-level triggering scheme

- T1 is formed by the programmable logic and causes the traces to be transferred to the ARM processor. The local T2 trigger is formed by software.
- The previous local triggers, threshold, and time-over-threshold (ToT) triggers are transferred to new electronics: compatibility triggers (40 MHz).
- WCD trigger is used for the readout of SSD and RD.
- New triggers (RD) are under development.

Compatibility triggers work, issues with ToTD and MOPS.

Implementation and interfaces

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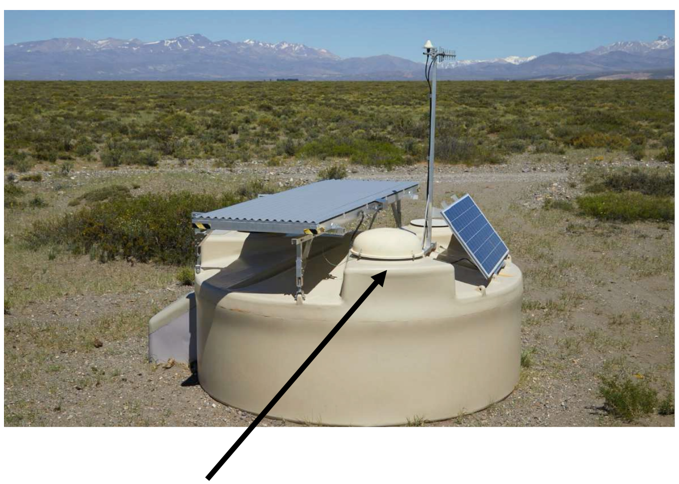
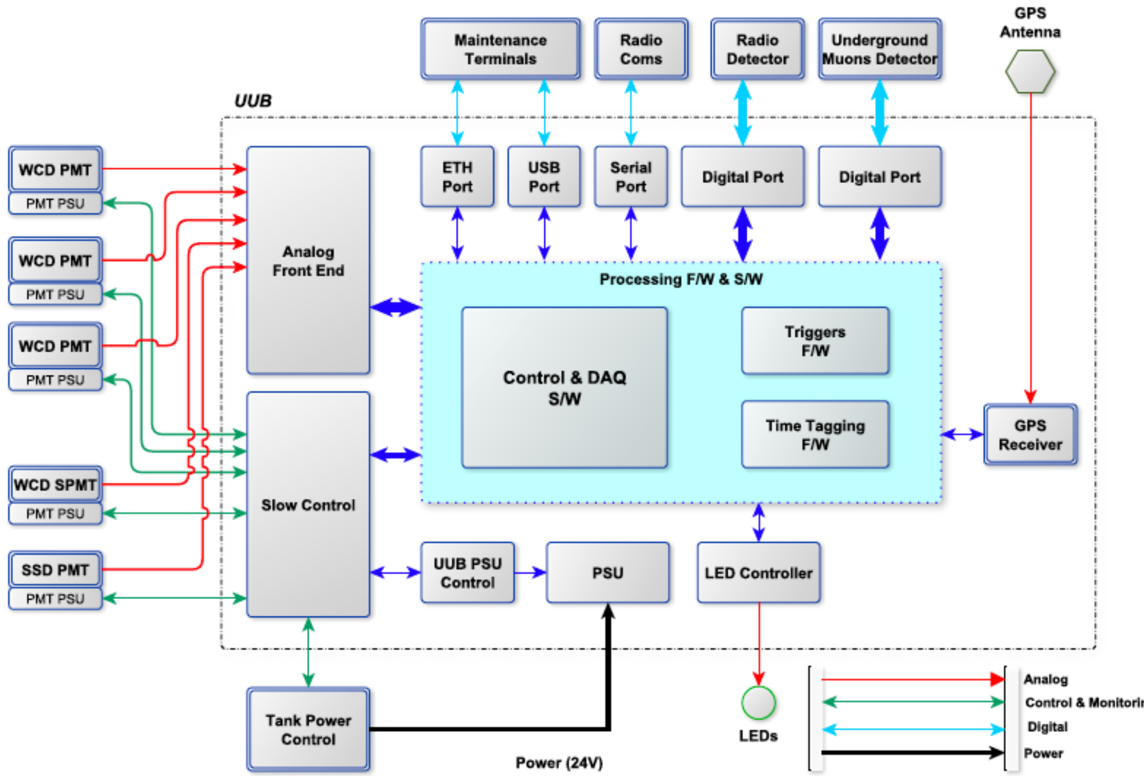
UUB



Electronics under a weather enclosure

Electrical interfaces of UUB

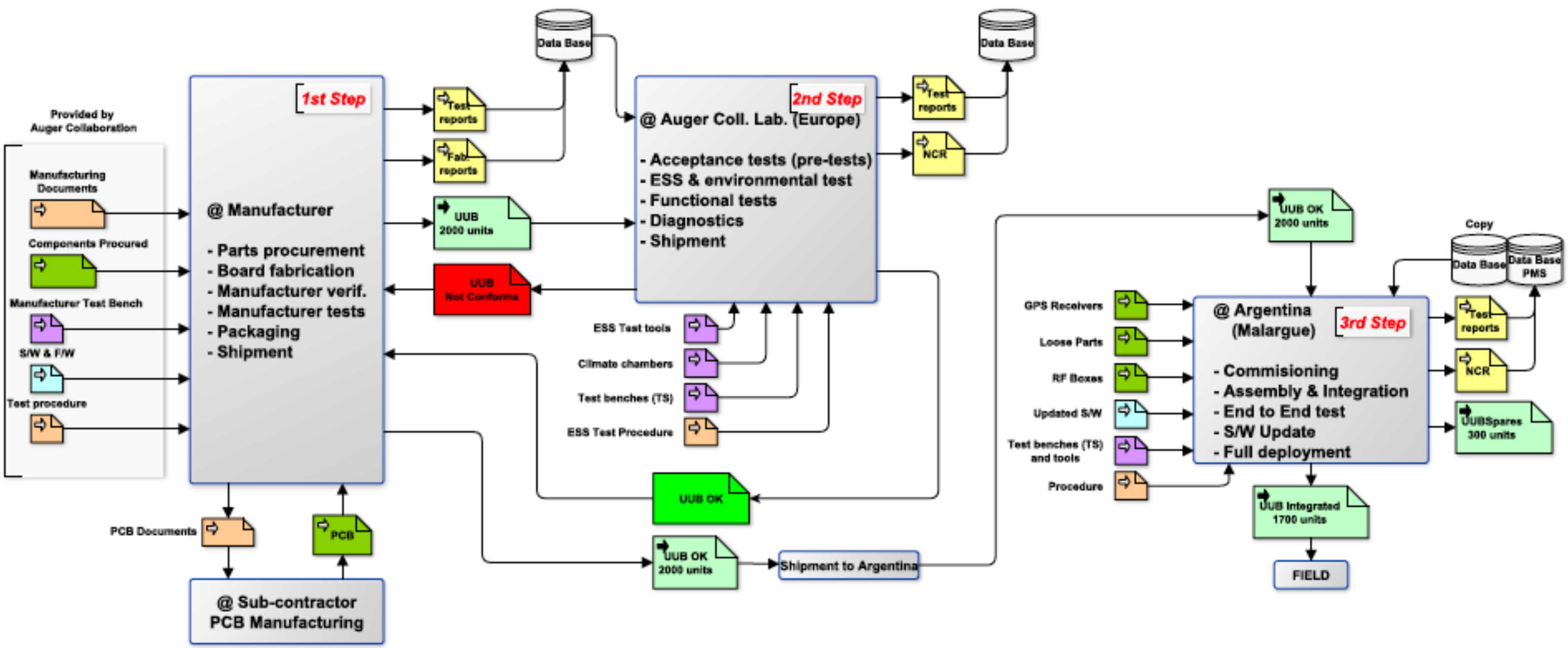


- All the functions except for the GPS receiver, on a single board of 340 mm × 215 mm size (UUB)
- UUB with the GPS receiver board mounted inside the existing metallic RF-proof enclosure
- Two 8-bit digital ports provided for additional detectors
- UUB interfaced with the actual communication system providing 1200 bps data transmission rate, and with the power system providing 24 V from the batteries

Interfaces have been tested and work.

UUB manufacturing and tests

- For manufacturing of 2000 UUBs the A4F company (Angel for Future, formerly SITAEL), Bari, Italy, was chosen.
- Currently, 1855 UUBs fabricated, tested, and shipped to Argentina
- Test procedure: manufacturing tests at A4F, Environmental and Stress Screening tests at Auger laboratory, assembly and final test at the Observatory before the deployment on site



Status of UUB manufacturing

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Inventory

Currently, 1855 UUBs are produced, tested, and shipped to Argentina (full array 1660).
145 UUBs still in Europe (2 golden samples, 1 UUB in Malargue)

- 44 working UUBs in Prague.
- A4F will ship 16 UUBs to Prague for ESS tests.
- A4F shipped 23 UUB to Kuttig (Germany) for component change (FPGA, memory) -> not back yet.
- A4F plans to ship 17 more UUBs to Kuttig for component change.
- 16 UUBs being investigated in A4F.
- 17 UUBs being reworked in A4F.
- 10 UUBs were rejected (<1%) for the moment. However, this rate is expected to increase since most of the remaining UUBs require repairing.

- **Regular meetings organised with A4F**
- **Minutes with actions and decisions**
- **Last meeting on 3 April :**

Actions :

- **Goal: Complete all activities in A4F and Prague by May 2024.**
- A4F will prepare a status report on the problem-solving activities.
- A4F will contact Kuttig to get their schedule for component changes.
- **A4F will prepare a schedule of their activities.**
- A4F should procure the lost SMA and 24V connector nuts and ship again these parts and ship them to Malargue.

General remark: Problems to get the schedule of A4F activities. Need to discuss actions to take concerning the schedule and the contract with A2F.

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Conclusions

- All UUBs have been manufactured, 1855 UUBs shipped to Argentina.
- UUBs with SSD PMT and SPMT have been deployed.
- More than 1600 detector stations are taking data.
- Performances meet the specifications.
- The commissioning of the AugerPrime is nearly completed.
- All documentation is stored (CERN EDMS and repositories).
- SDEU paper has been published: 2023_JINST_18_P10016,

http://arxiv.org/abs/2309.06235
https://doi.org/10.1088/1748-0221/18/10/P10016

- **Need to solve the issue with the A4F schedule.**

Presentations

Documentation, Patrick Stassi (5 min)
UUB Commissioning, Martin Schimassek (20 min)
UUB Hardware failures, spares, and maintenance, Patrick Stassi (20)
Firmware/software status, Dave Nitz (20 min)
SPMT status, Antonella Castellina (30 min)

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Backup slides

Requirements for UUB

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Functional requirements

- 10 ADC analog inputs to handle the two gains for each of the three existing PMTs, the added PMT of the SSD detector and the SPMT (plus a spare channel).
- The total RMS integrated noise at the ADC input should not exceed 0.5 LSB (Least Significant Bit) for the low-gain channel and 2 LSB for the high-gain channel.
- Digitization of the PMTs anode signals at a sampling frequency of 120 MS/s with a resolution of 12 bit minimum.
- Existing and additional trigger configurations implemented in the FPGA firmware.
- Event time tagging with a resolution of 5 ns with a stability better than 5% depending on temperature variation.
- Independent programmable Slow-Control unit to monitor voltage and environmental sensors, and control the PMT high voltages and the FPGA low voltages.

Configuration requirements

- All functions contained on a single board (except for the GPS receiver).
- Use of up to date commercial GPS receivers.
- Embedded diagnostics.
- Digital ports allowing communication with additional detector systems.
- Power-supply unit including safety features and an efficiency better than 80% for a total consumption between 10 and 11 W.

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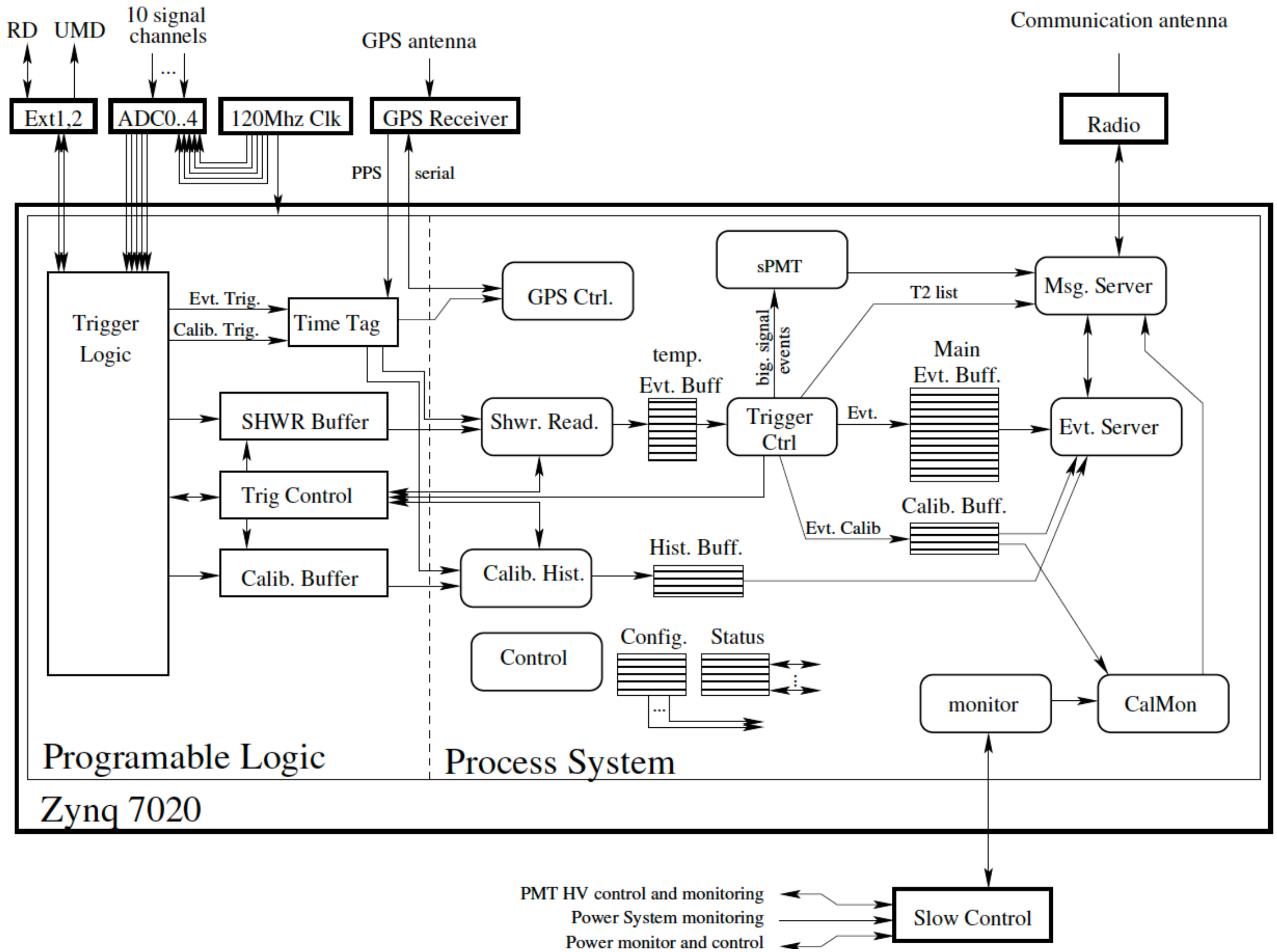
Commissioning

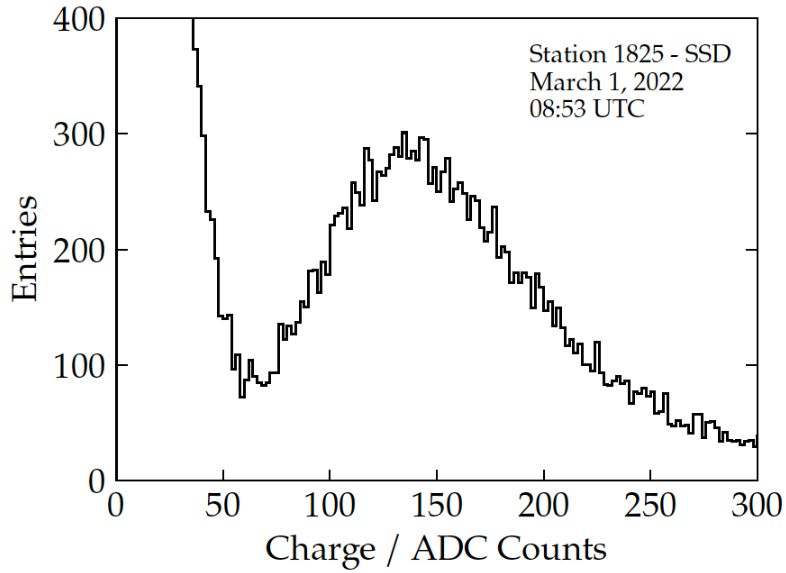
- SDEU Commissioning in progress since the end of 2020
  - Meetings every 2 weeks, minutes of the meetings on Wiki:
    https://www.auger.unam.mx/AugerWiki/SDEU_Front_Page
- Stable and uniform performance
- RD and UMD interfaces tested and work
- COMMS works, both regular array with the current radio and infill with UMD COMMS
- SPMT commissioned (HV setting, cross-calibration, data flow)
- Rates of downscaled basic triggers similar to those of previous UB triggers (ToT 1 Hz and T2 20 Hz)
- UUB T2 trigger time adjusted to UB T2 allowing observation of hybrid events
- GPS 1-second offset problem mitigated by modification of the GPS initialization software
- Some noise issues observed in the field (related to the power system, bad grounding, and lightning), currently being mitigated
- Taking data with more than 1600 detector stations, Local Station efficiency end of October: 98,6%

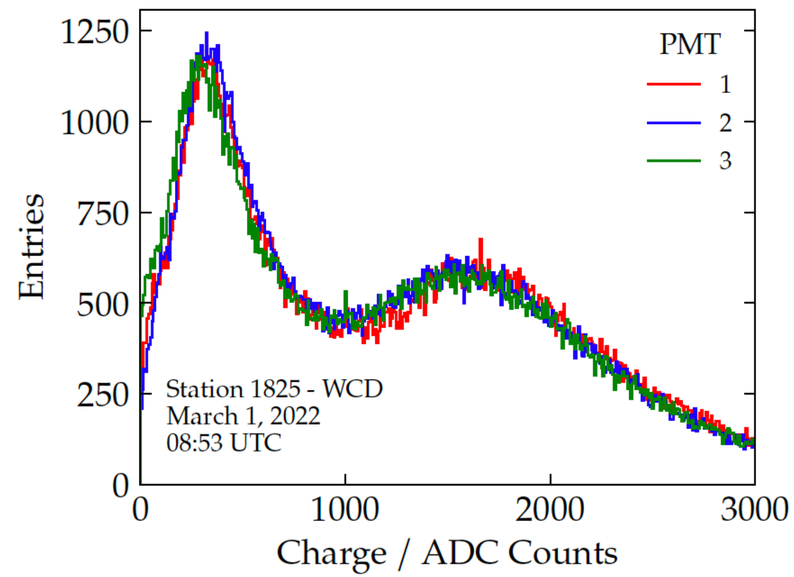
Local Station Software



Block diagram of local processing Software. The rounded corner blocks are the processes that run on the operating system.

Calibration





WCD is calibrated by Vertical Equal Muons (VEM).
SSD is calibrated by Minimum Ionizing Particle (MIP).

A dedicated selection of small local shower events is exploited to cross-calibrate the SPMT using the VEM-calibrated signals of the WCD PMTs.