Electronics plans

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- Transformative **discovery in science** is driven by **innovation in technology**. This mean that our boldest undertakinkgs in particle physics **have at their foundation precision instrumentation.**

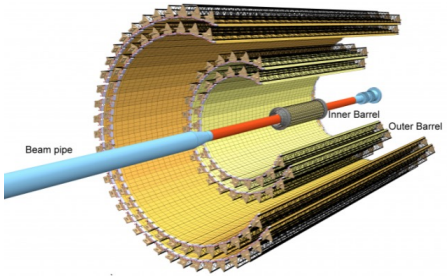
- We are firmly conviced that to reveal the profound connections underlying everything we see from the smallest scales to largest distance of the universe, to understand its fundamental constituents, and **to reveal what is still unknow**, **we must invent, develop and deploy advanced instrumentation.**

Introduction

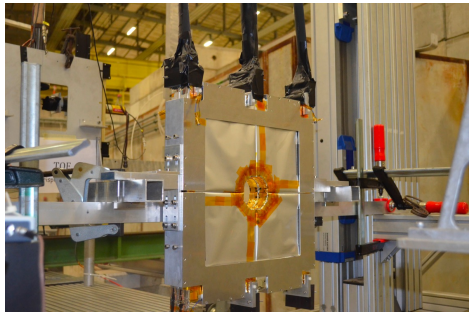
- ACORDE

- TPC

- ITS Upgrade

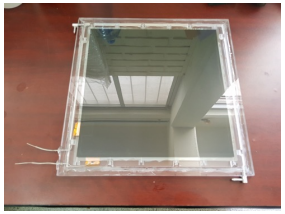


- BELLE II (LABM)

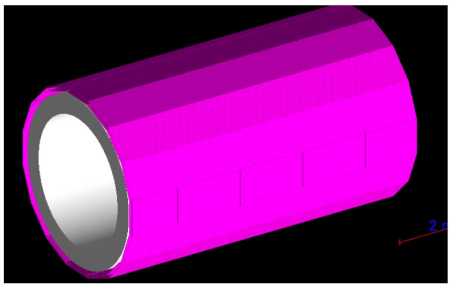


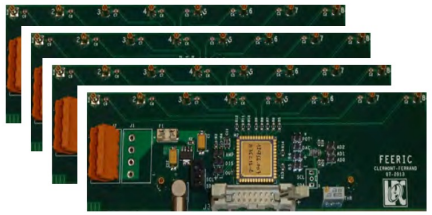
FDD

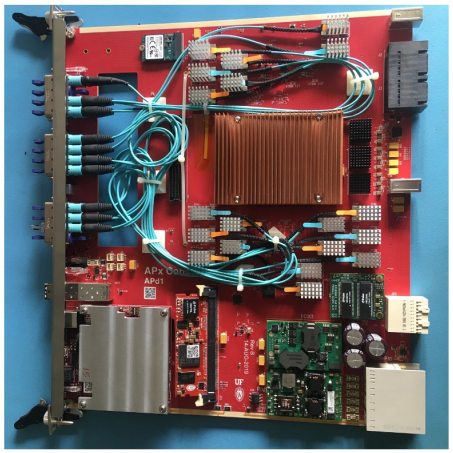
CTP

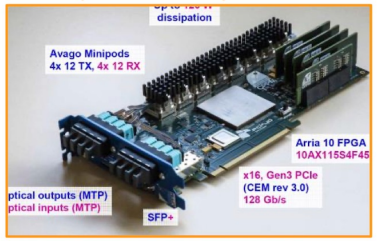


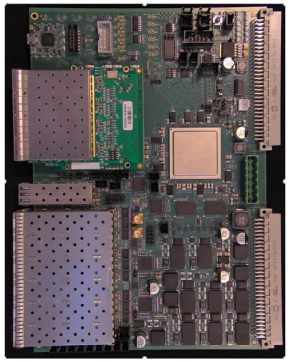
Introduction (Associated Electronics to High Energy Experiment)











Detector

Front End Electronics
- ASICS
- Higher Radition Levels

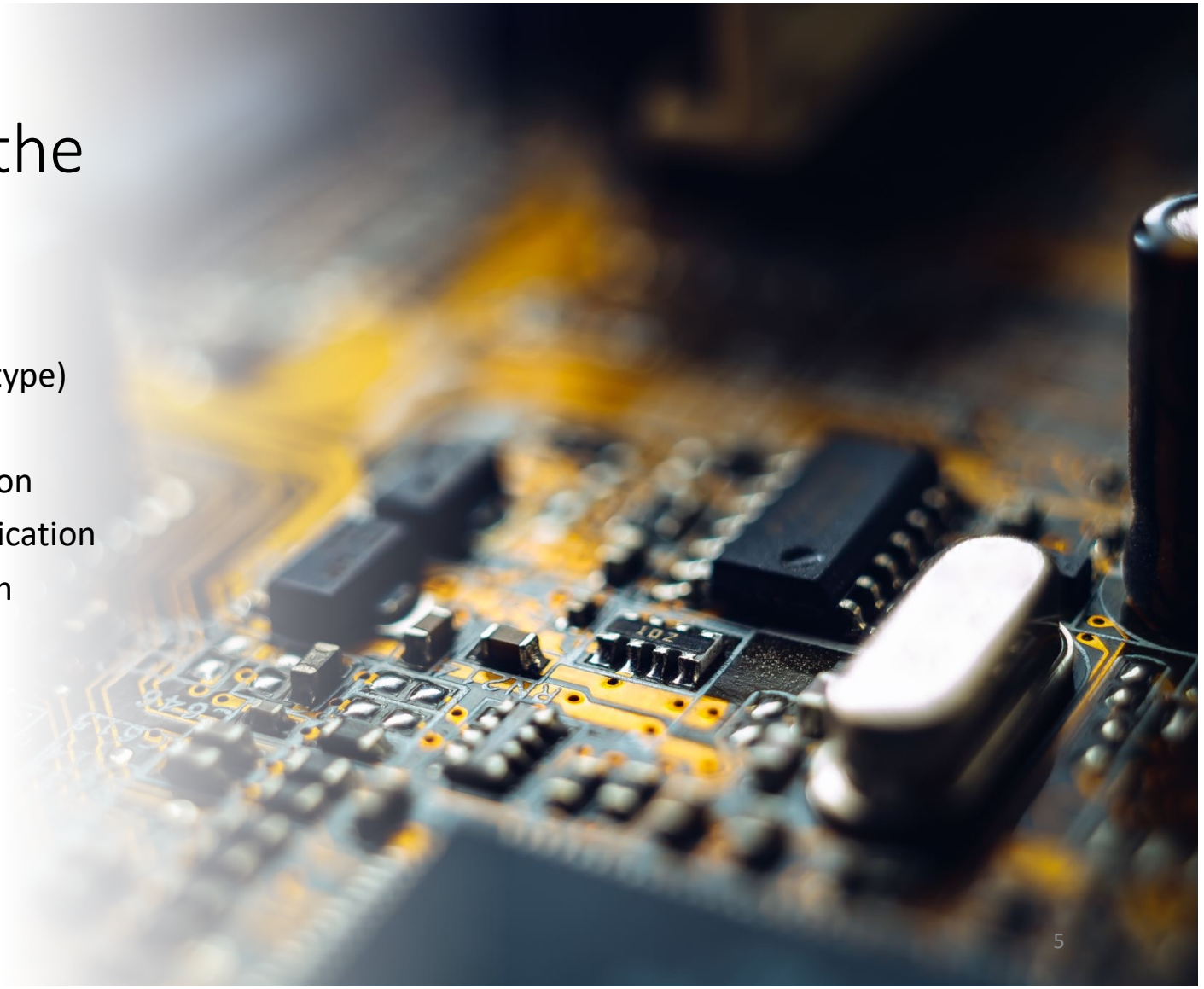
Back End Electronics
- **FPGA**
- Standalone DAQ (Test beam)
- Lower Radiation Levels

Central System
- Trigger / DAQ/DCS

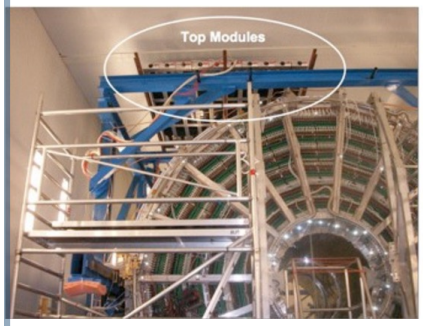
Electronics in the detector

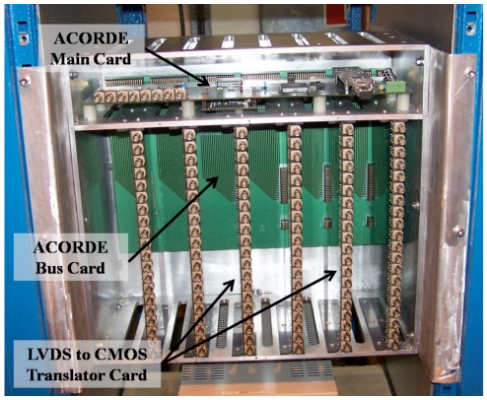
- FEE (depend on detector type)
- ReadOut
- DAQ system communication
- TRIGGER system communication
- Debugging communication
- Power Supply
- Cabling
- Cooling

- DCS interfce



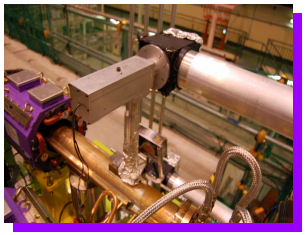
ACORDE





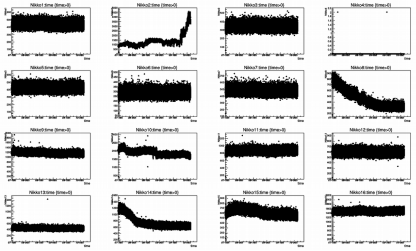
LABM

Optical Chanels

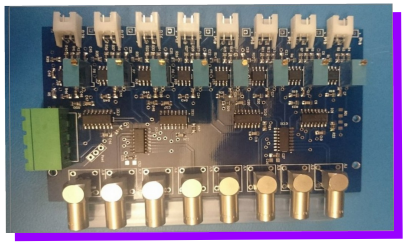


Mirrors remotely controled

HV, LV and counters

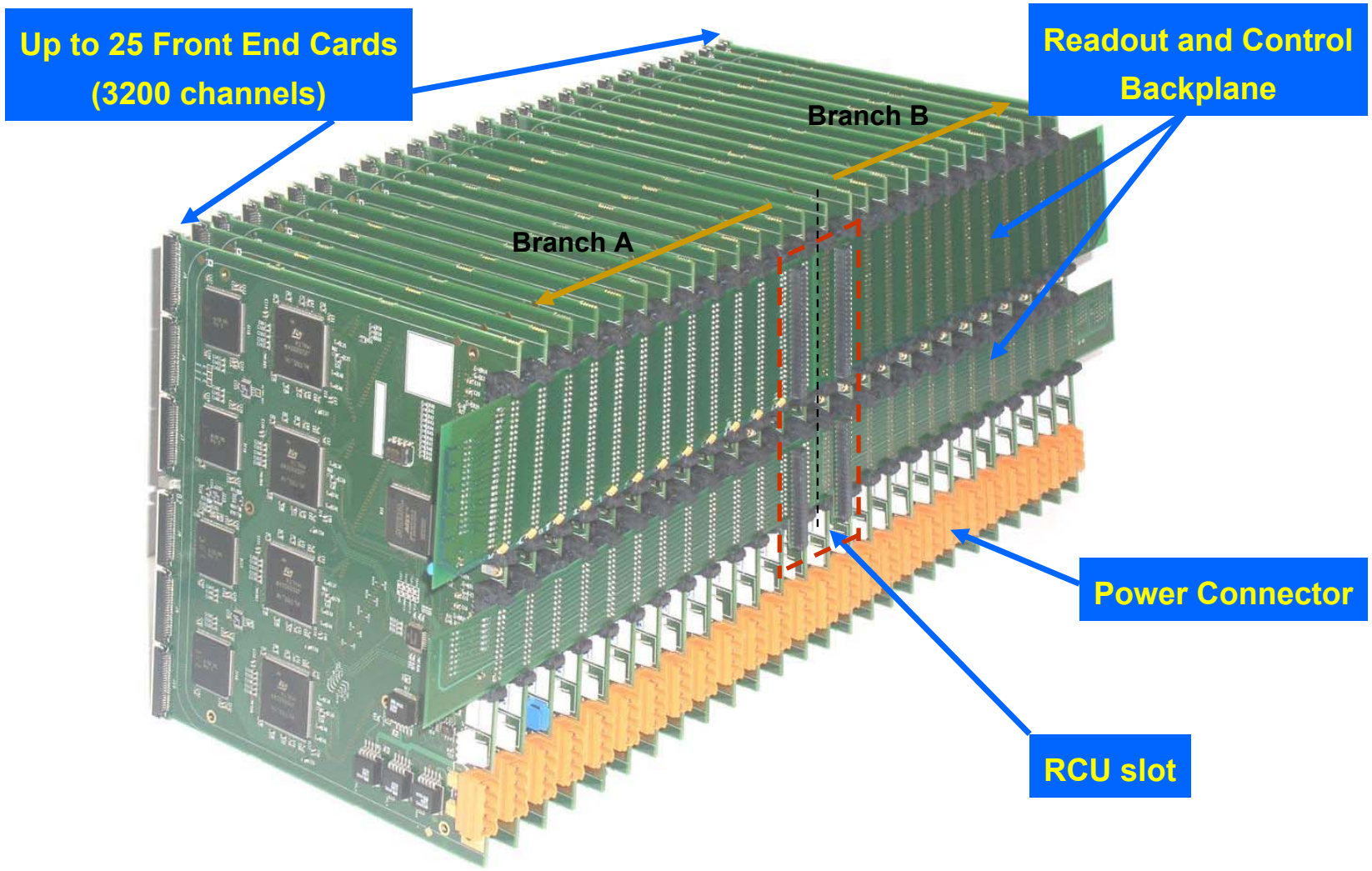


Data



Electronic card

Readout Backplane – example of readout partition



RPC FEE

First proto

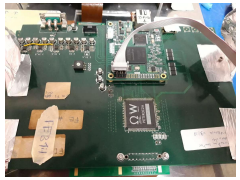
2017
proof of principle for
CMS-MUON-TDR-016

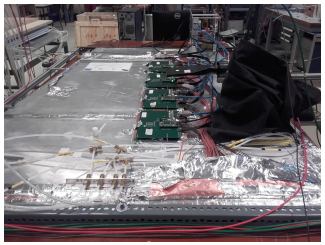
2 PetiROC2A
+ FPGA Cyclone II
+ ETHERNET
directly on strip PCB
(50 cm)

Feb V0

2018
First FEB (Conf. note)

1 PetiROC2A +
MEZZANINE with
FPGA Cyclone II
+ ETHERNET





Feb V1

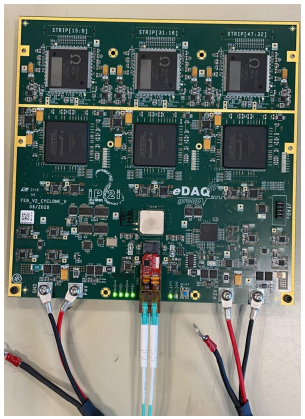
2019
FEB without
mezzanine

2 PetiROC2B
+ FPGA Cyclone V
+ ETHERNET

Feb V2

2021
Non-rad hard
for iRPC Demo

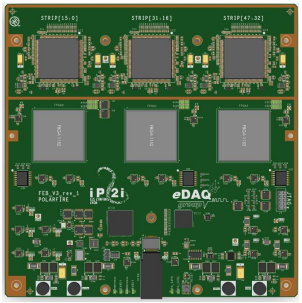
6 PETIROC2C
+ 3 FPGA Cyclone V
+ Optical GBT



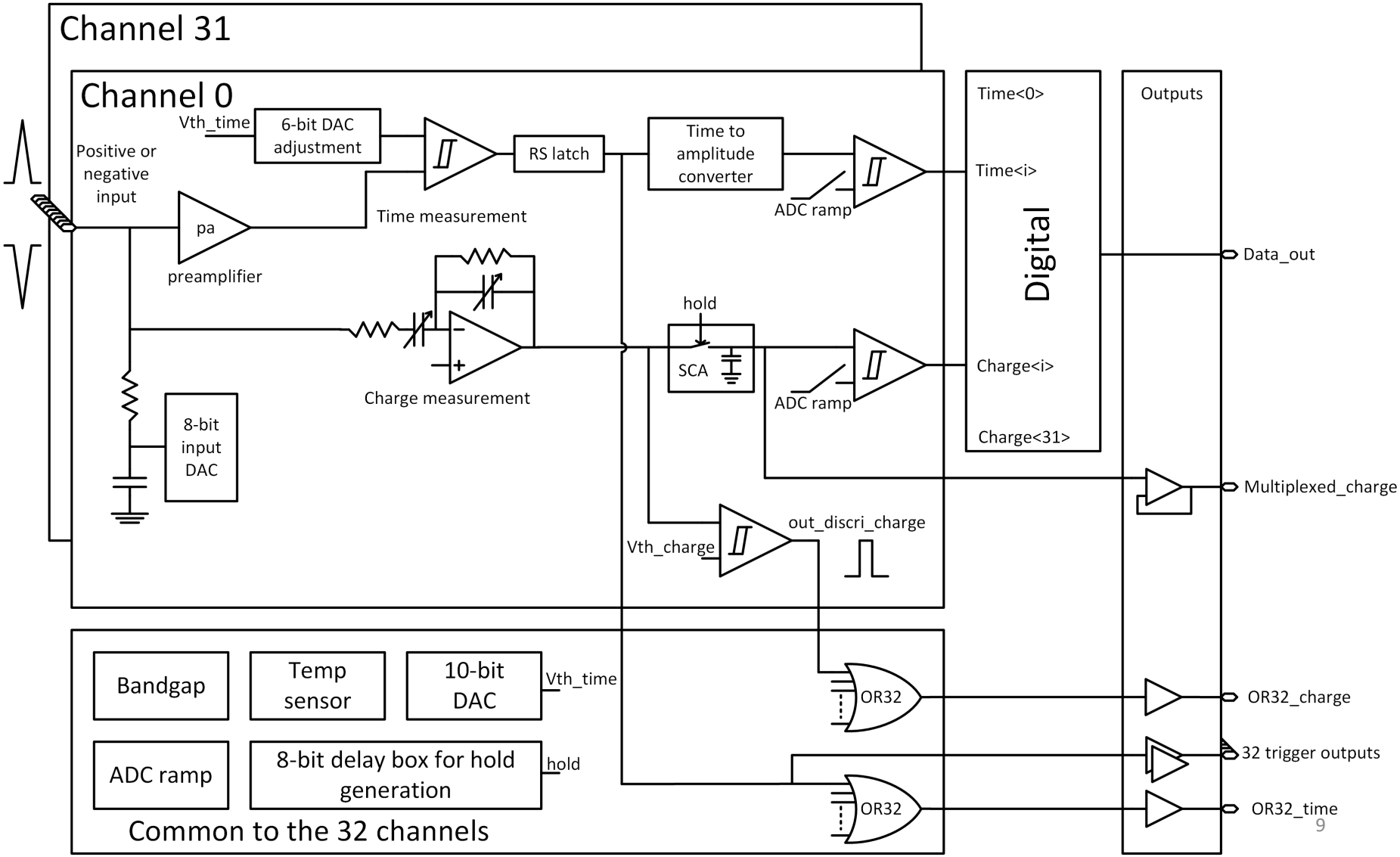
Feb V3

→ 2023
Rad hard
final

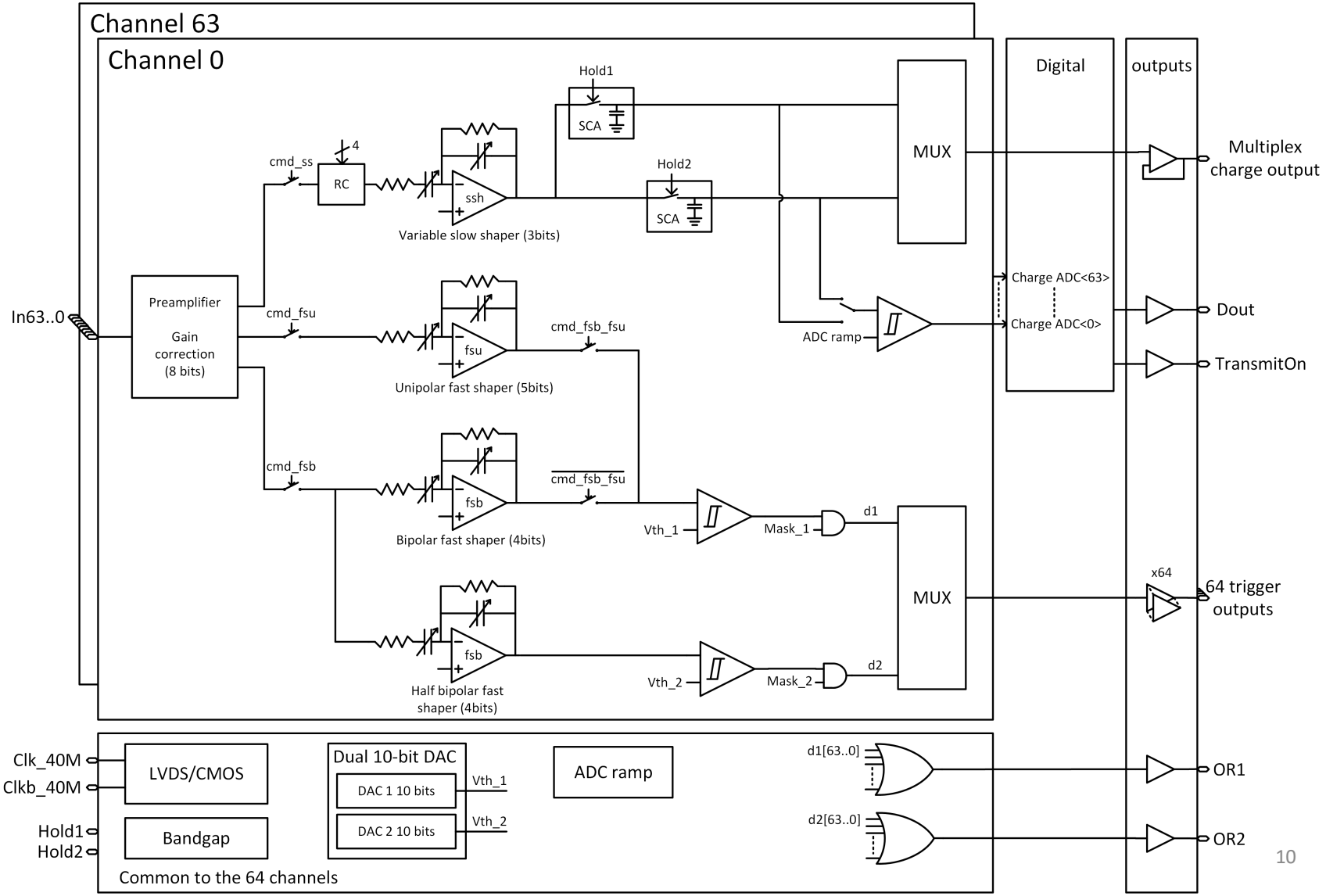
6 PETIROC2C
+ 3 FPGA PolarFire
+ Optical GBT



Petiroc 2C (RPC)



MAROC 3A (PMT)


Channel 63
Channel 0
Digital
outputs
Hold1
SCA
Hold2
SCA
MUX
Multiplex
charge output
cmd_ss
4
RC
ssh
Variable slow shaper (3bits)
In63..0
Preamplifier
Gain
correction
(8 bits)
cmd_fsu
fsu
cmd_fsb_fsu
Unipolar fast shaper (5bits)
ADC ramp
Charge ADC<63>
Charge ADC<0>
Dout
TransmitOn
cmd_fsb
fsb
cmd_fsb_fsu
Bipolar fast shaper (4bits)
Vth_1
Mask_1
d1
MUX
x64
64 trigger
outputs
fsb
Half bipolar fast
shaper (4bits)
Vth_2
Mask_2
d2
Clk_40M
Clkb_40M
LVDS/CMOS
Hold1
Hold2
Bandgap
Dual 10-bit DAC
DAC 1 10 bits
DAC 2 10 bits
Vth_1
Vth_2
ADC ramp
d1[63..0]
d2[63..0]
OR1
OR2
Common to the 64 channels

Channels distributions example

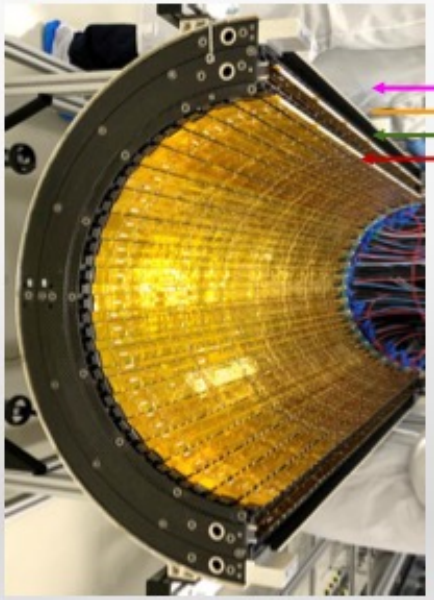
- 13500 Channels

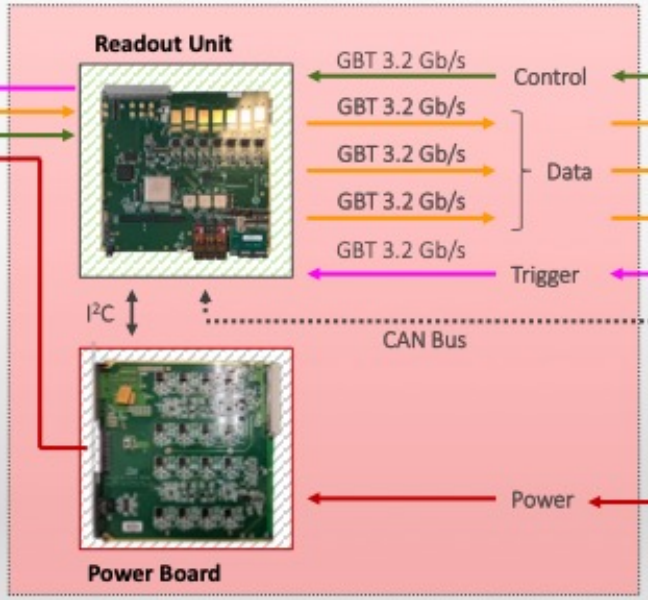
RPC:
422 PETIROC chips
104 FEE cards with 4 chips (128Ch/card)
13 CRU with 8 FEE connected

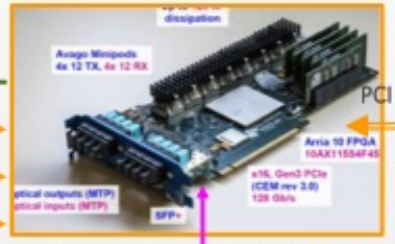
PMT or SiPM:
211 MAROC chips
53 FEE cards with 4 chips (256 Ch/card)
7 CRU with 8 FEE connected

Equivalent for PicoTDC.

- The ITS Front End Electronic (FEE) is divided into modular Readout Units (RU), identical for each layer.
- Each readout unit controls an entire stave, including power to the sensors (through custom-made Power Boards).
- The experiment DAQ, Trigger and Control interfaces with the RU only through the Common Readout Unit.







Common Readout Unit (CRU) is optically (GBT) connected to the ITS front-end electronics. Performs DAQ, slow control and DCS.
Each CRU controls more than one RU.

The O² system performs DAQ, data packaging/clustering and broadcasts control (DCS).

Central Trigger Processor (CTP) optically connects to the ITS via dedicated GBT link

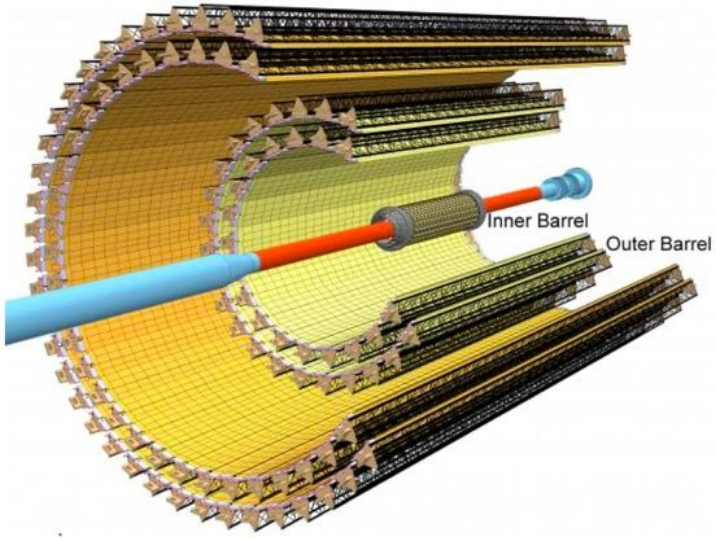
Power

CAEN

The DCS has two paths toward/from the ITS: the main one through the O²/CRU via the optical connections used also for data shipping, the other backup through the CAN bus used to monitor/control the power supplies.

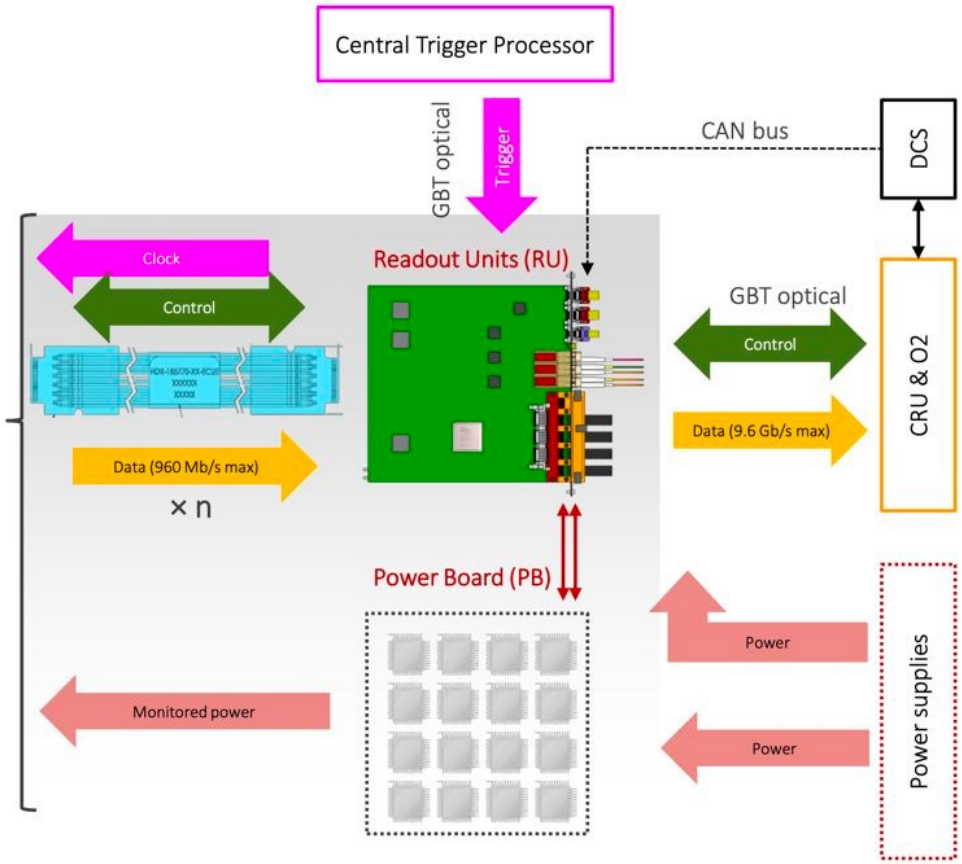
Specifications – ITS Readout Electronics is organized in Readout Units (RU)

The ITS front-end electronics are divided into **192** modular **Readout Units**, each connected to one ITS stave, and optically interfaced with both the Common Readout Unit (CRU) and the Central Trigger Processor (CTP).

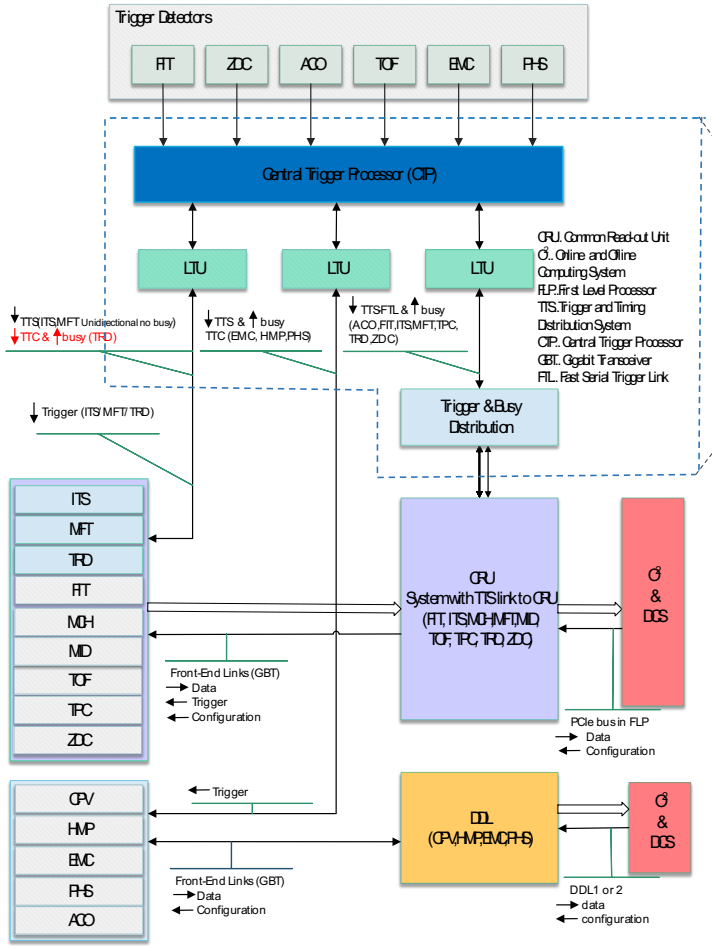


Each Readout Unit is connected to one stave,
both for Inner and Outer Barrels

× 192 staves



CTP Requirements for LHC-Run3



>> Select different physics

>> Different trigger detectors
--- (ACO, FIT, EMC, PHOS, TOF, ZDC).

>> Optimize for different running scenarios

>> pp, pA , AA collisions, with different interaction rates

>> Optimize use of detectors with

>> Continuous readout.
>> Widely different busy times.
>> Different latency times.
>> Different Technologies (TTC, GBT, TTC-PON)

>> Special triggers

>> Calibration, Control, debugging..

>> BUSY handling

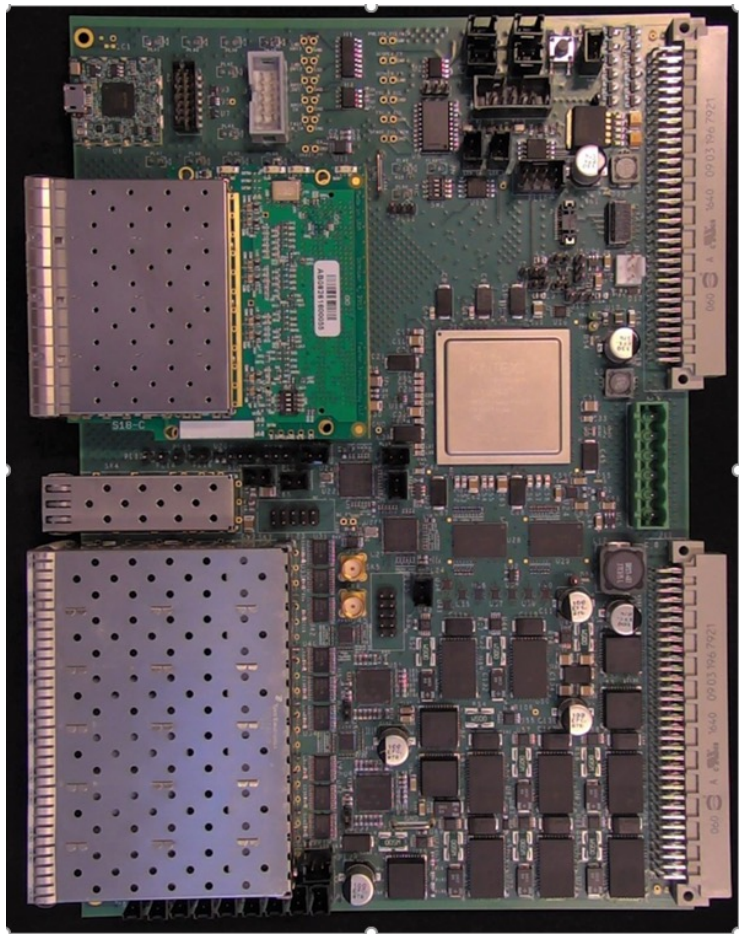
>> Busy propagated with minimal latency.
>> Busy for Upgrade & non Upgrade detectors .

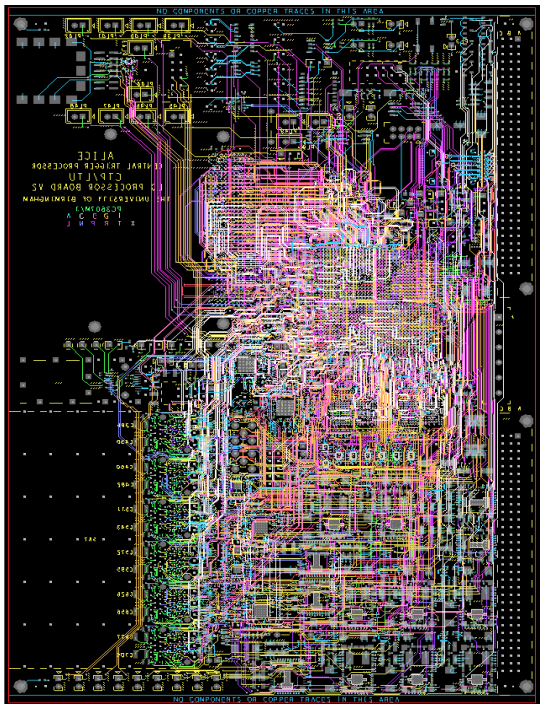
Block Diagram ALICE – Run 3

OLT: Optical Line Terminal
ONU: Optical Network Unit

ALICE CTP Requirements

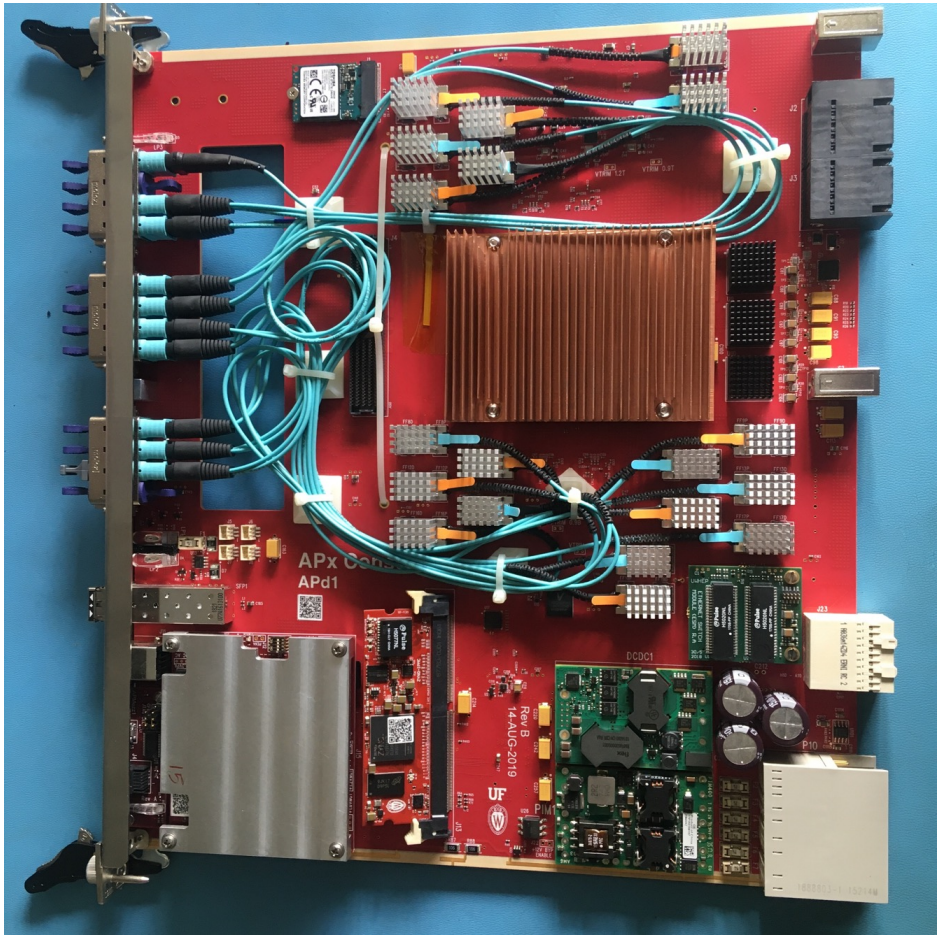
ALICE Trigger board for LHC-Run3





- **Kintex-Ultrascale FPGA**
- Single universal trigger board (CTP/LTU board).
- **Interface between CTP and LTUs is via TTC-PON and optical fan-out unit.**
- Will still be based on a VME-type 6u board (VME for power only).
- **PCB design**
  *** 20 Layers (I-TERA MT40 material for high-speed digital multilayer)**
  - **All clocks have the same length**
- **2GB DDR4 Memory**
- **2 Synthesizers**
- **20 Optical Links (up to 11 Gbps)**

Advance Processor board (CMS-Level 1 -- HL- LHC)



- APx- Family card for Phase 2 Trigger:
  Calorimeter, Correlator Muon.

- Demonstrator for a multi-purpose, customizable, common processing platform, suitable for wide-scale use in CMS back-end trigger subsystems.

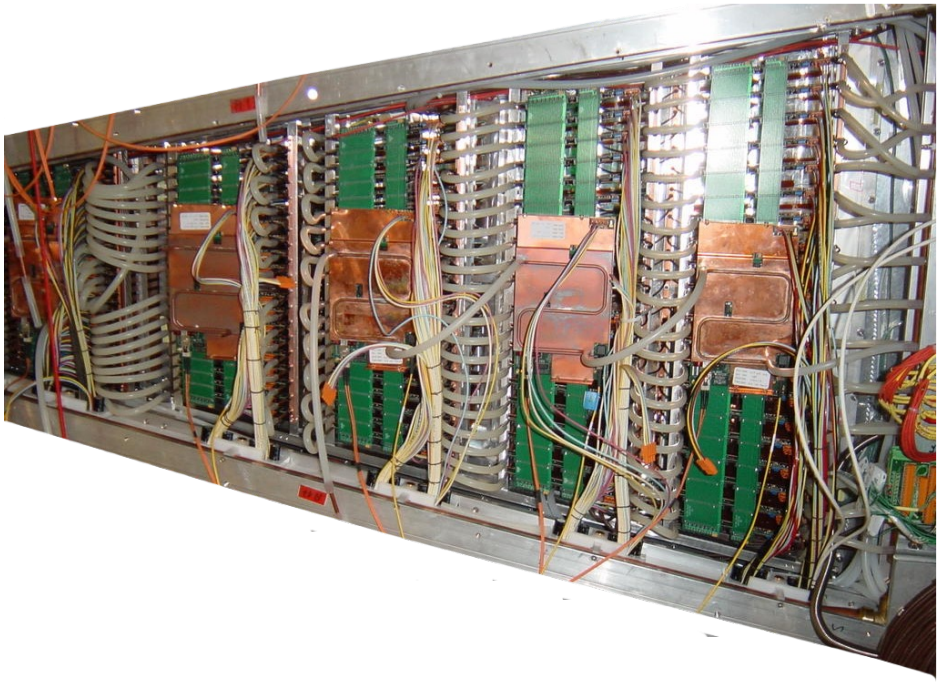
- **Virtex Ultrascale+ FPGA**
- Flexible and expandible
- Control via ZYNQ SoC (ELM1 Embedded Linx Mezznine)
- Based on ATCA standard

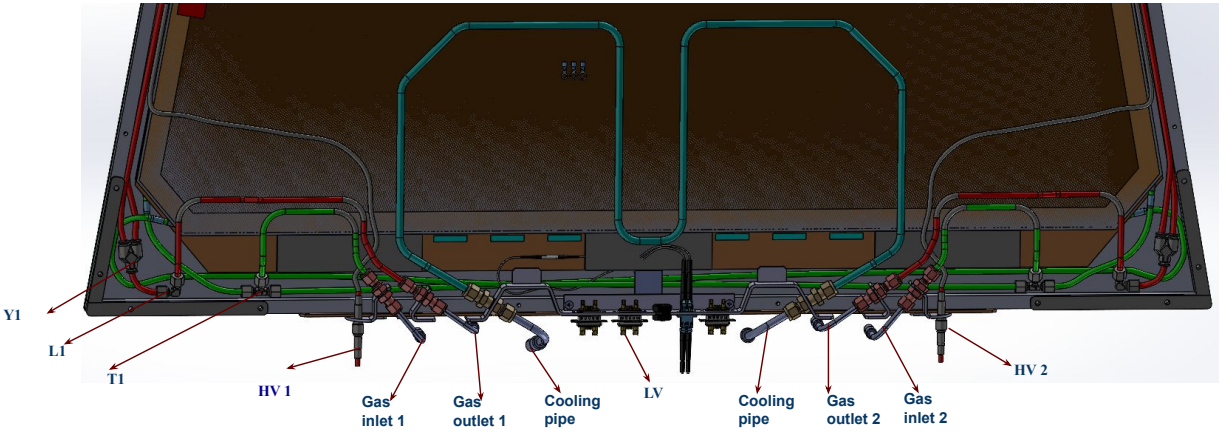
- **PCB design**
  *** 20 Layers (I-TERA MT40 material for high-speed digital multilayer)**

- **~ 100 Rx/Tx Optical links (28 Gbps)**
- **4 Synthesizers**
- **2 Retimers Chips**
- **10GbE ELM connection supported via SFP**

cooling

TPC





RPC gas and cooling

Electronic system tasks

- Design of the FEE for RPCs, PMTs or SiPM.
- Design of the Read Out Unit for the FEE.
- Design of the DCS and electronics communications.
- Design of the trigger and control modules.
- Design of the DAQ system communication.

Experience in electronics

- Dr. Luis Alberto Perez Moreno
- Guillermo Tejeda Muñoz
- David Regules Medel
- Yael Antonio Vasquez Beltran
- Emigdio Jimenez Dominguez
- Omar Mancilla Martinez

Thank You