

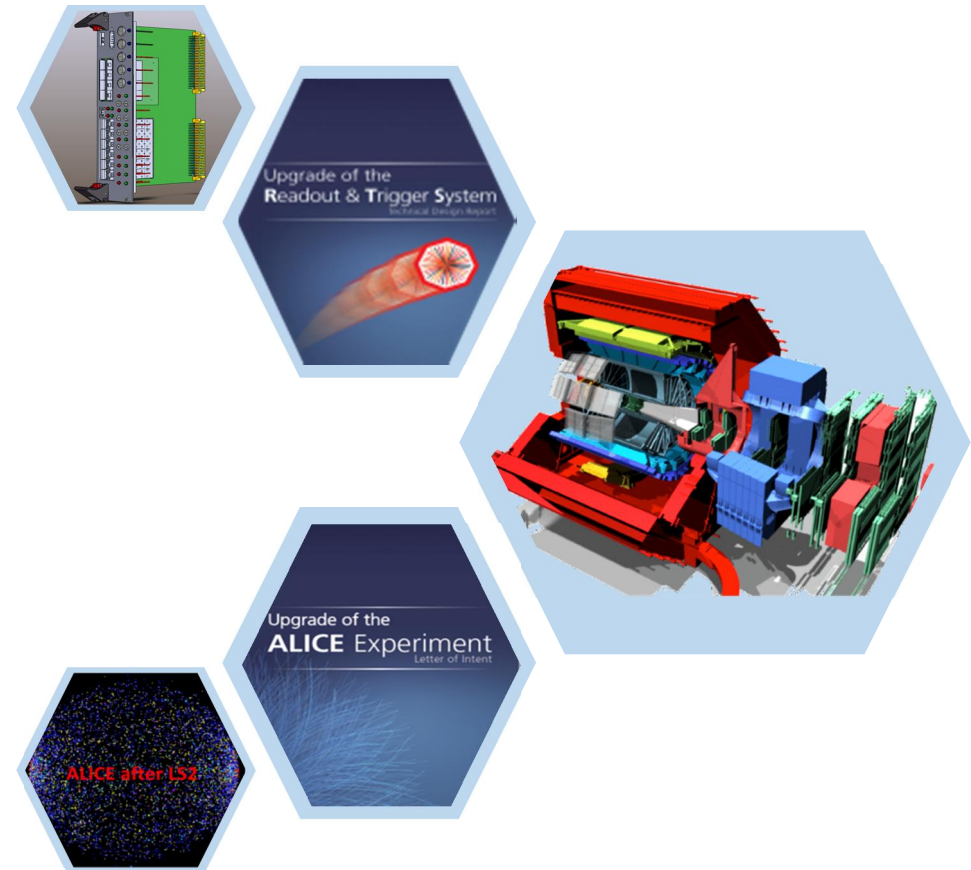


# Diseño e implementación de criterios físicos para la selección de eventos en el experimento ALICE-LHC del CERN

Tercer Avance de Tesis

Alumno:  
**Luis Alberto Pérez Moreno**

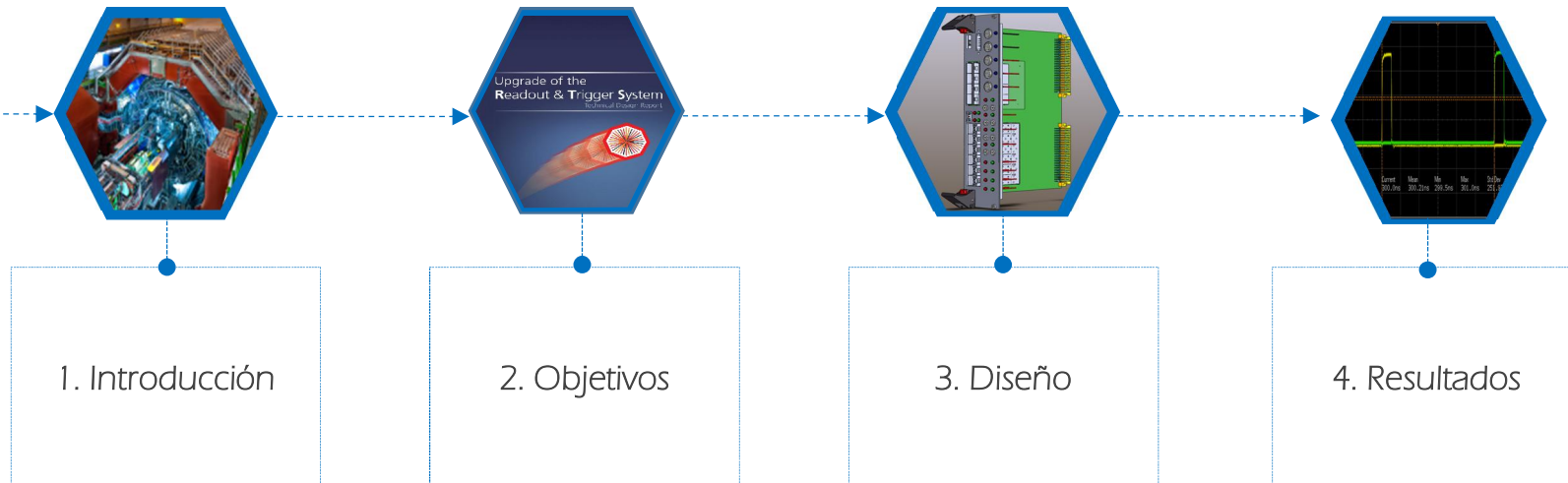
Asesores:  
Dr. Arturo Fernández Téllez  
Dr. Guillermo Tejeda Muñoz



# ► The ALICE Central Trigger Processor (CTP) for Run 3



## ► Contenido





### ALICE

El propósito general del Experimento ALICE es estudiar las colisiones de iones pesados, enfocándose principalmente en fenómenos de QCD en un medio de materia de deconfinada, en particular en el estudio de las **propiedades del Plasma de Quark y Gluones (QGP)**.

### Motivación

ALICE se centrará en **mediciones de alta precisión** (en eventos de medio y bajo  $p_T$ .)

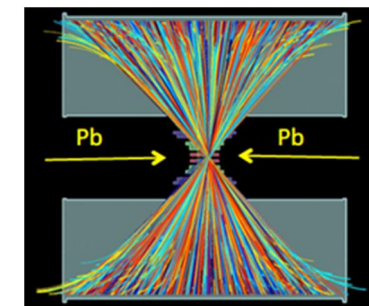
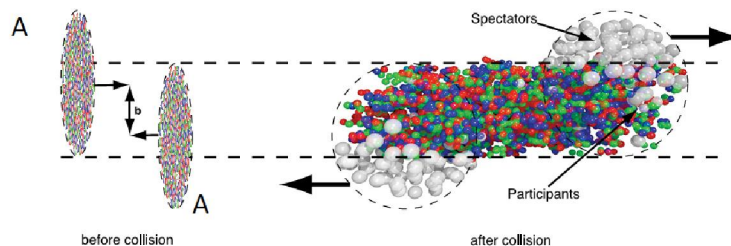
- Es necesario **colectar la mayor cantidad de información.**

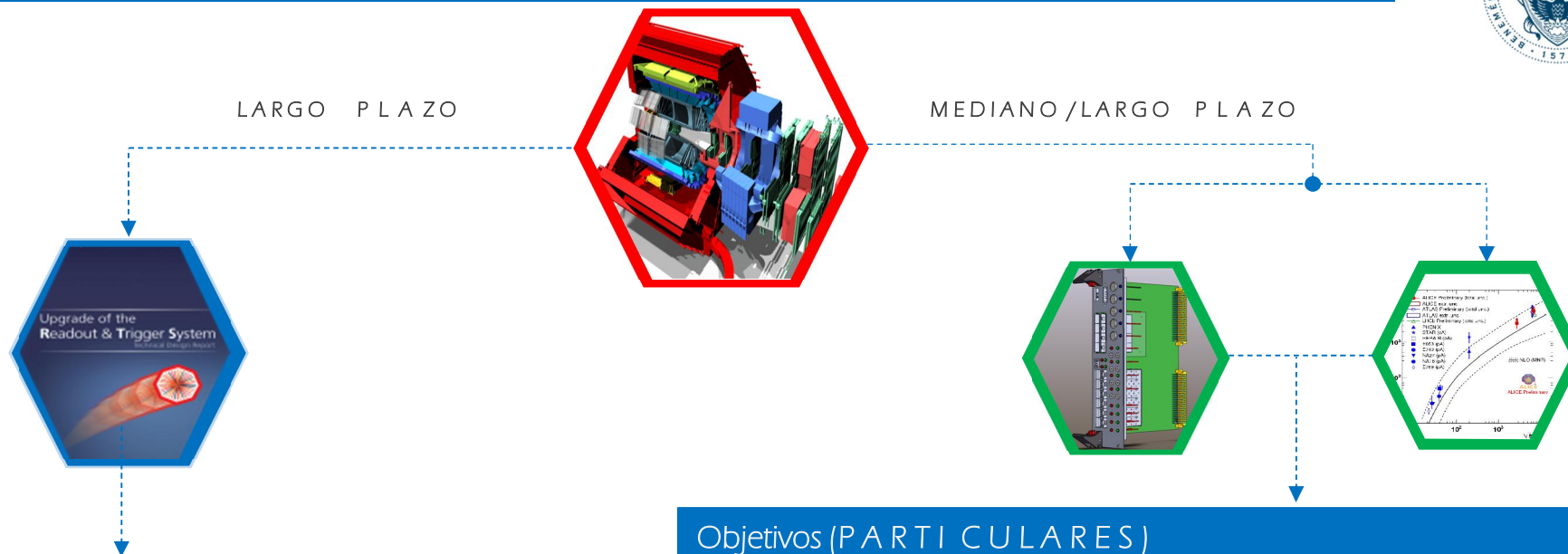
### Escenario

- Pb-Pb recorded luminosity:  $\geq 10 \text{ nb}^{-1} \rightarrow 8 \times 10^{10}$  eventos.
- pp(@ 5.5 Tev) recorded luminosity  $\geq 6 \text{ pb}^{-1} \rightarrow 1.4 \times 10^{11}$  eventos
- Minimum bias physics: **gain a factor 100**
- Triggered physics: **gain factor 10**

### Estrategia

- Actualización en los sistemas de lectura de algunos detectores de ALICE (TPC, muons).
- Actualización de los sistemas centrales de ALICE (**CTP & DAQ**).
- Actualización del detector Interno de Trazas (ITS)





## Objetivo (GENERAL)

- Optimización del sistema central de disparo (CTP) del experimento ALICE-LHC del CERN.

## Objetivos (PARTICULARES)

- Estudiar las especificaciones que debe de cumplir el CTP-ALICE para el periodo de toma de datos denominado LHC-Run3.
- Diseñar, construir e implementar el nuevo CTP-ALICE.
- Instalación y pruebas de funcionamiento.
- Analizar comportamiento/variaciones de la Luminosidad instantánea que proporciona el LHC en el IP (Interaction Point de ALICE) en el calculo de las secciones eficaces elástica, inelástica, difractiva.

# Plan de Trabajo.

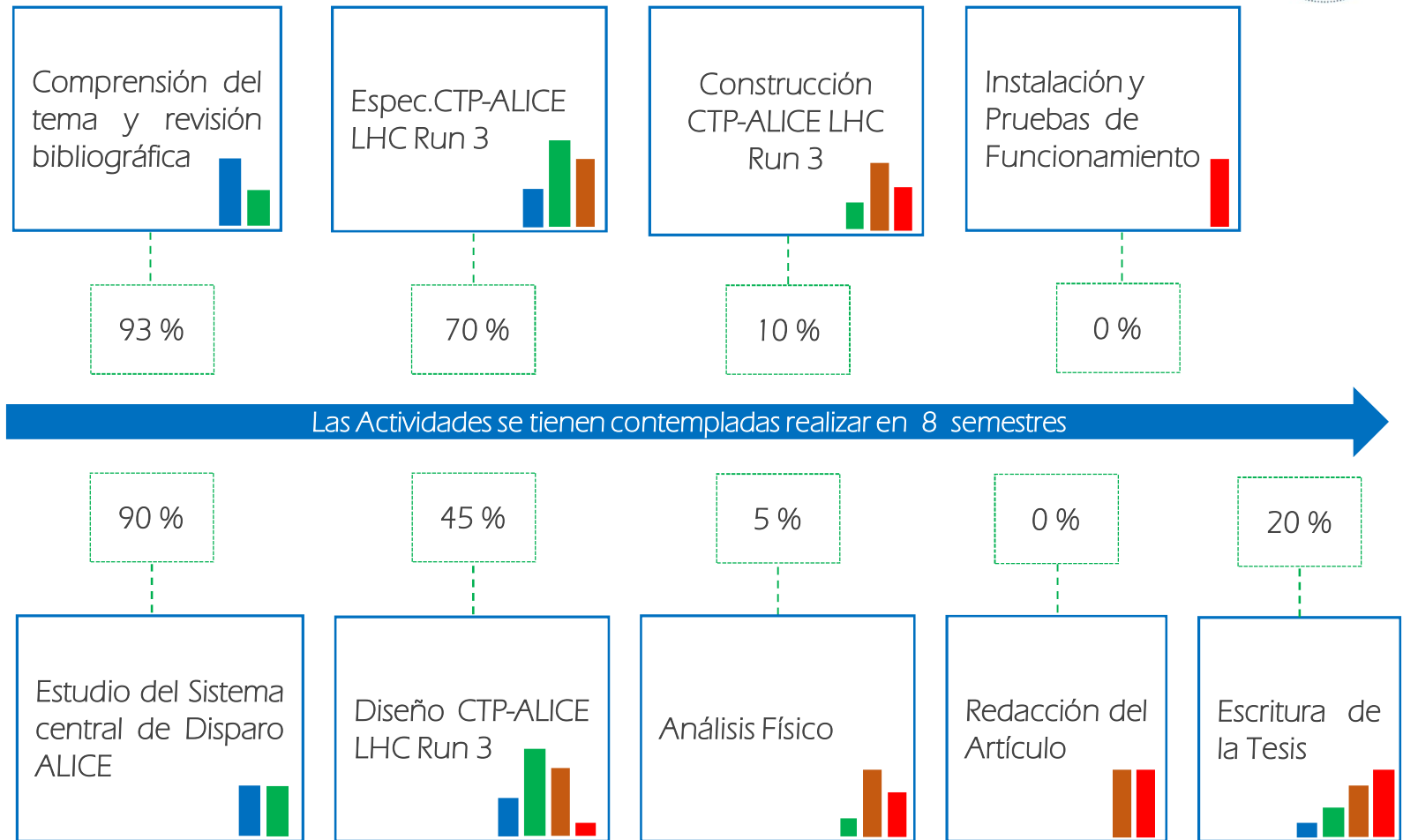


**INICIO**

Enero/ 2015

---

Planteamiento del problema, Estado del arte.



- Avance Actual.
- Semestre ( 1 – 2 ).
- Semestre ( 3 – 4 ).
- Semestre ( 5 – 6 ).
- Semestre ( 7 – 8 ).

\*Nota: El plan de trabajo o sus actividades pueden ser modificados, durante el desarrollo de la tesis, de acuerdo a criterios confidenciales de los asesores, alumno o colaboración.

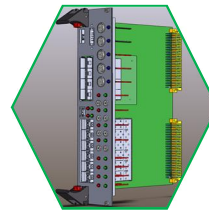


**Diseño y Construcción de las CTP-b y LTU-b. | 40 %**

- Presentación en ALICE System Forum
- Diseño del CTP-b y LTU-b
- Colaboración, en la escritura del TDR

**Diseño e implementación del firmware del LTU | 60 %**

- i2c (Configuración del reloj)
- IPbus (Control y Monitoreo)
- GBT y 10G PON (Comunicación con detectores y CRU)



2016

(Objetivo Principal)  
Diseño y construcción  
del Local Trigger Unit

**Definición de un análisis físico | 30 %**

- Análisis con la información del CTP.
- Revisión de literatura.

**Diseño e implementación del Emulador del CTP | 40 %**

- Interfaz gráfica (IPbus – ftk)
- Definición de los tipos de disparo .
- Definición de los mensajes de disparo.
- Transmisión en paralelo GBT y 10G PON



TDR (CTP-Upgrade) → En proceso

# Trigger System Design Review

May 2016

D. Evans<sup>1</sup>, A. Jusko<sup>1</sup>, M. Krivda,<sup>1</sup> L. Lietava<sup>1</sup>, L. A. Perez Moreno<sup>2</sup>

O. Villalobos Baillie<sup>1</sup>

1. University of Birmingham

2.-Autonomous University of Puebla

Version 2.0

May 2016



El trabajo realizado se reporta continuamente en:

- CTP- Upgrade (CERN)
- (ACORDE-Puebla) (A. Fernández)



Reporte de Actividades

Luis Alberto Pérez Moreno – BUAP

Outline

- ▶ CTP-Emulator (Data Frames)
- ▶ FPGA\_GBT 4\_0\_0

ACORDE – Puebla Meeting

21 – May – 2016



ALICE



CTP-Emulator (Status)

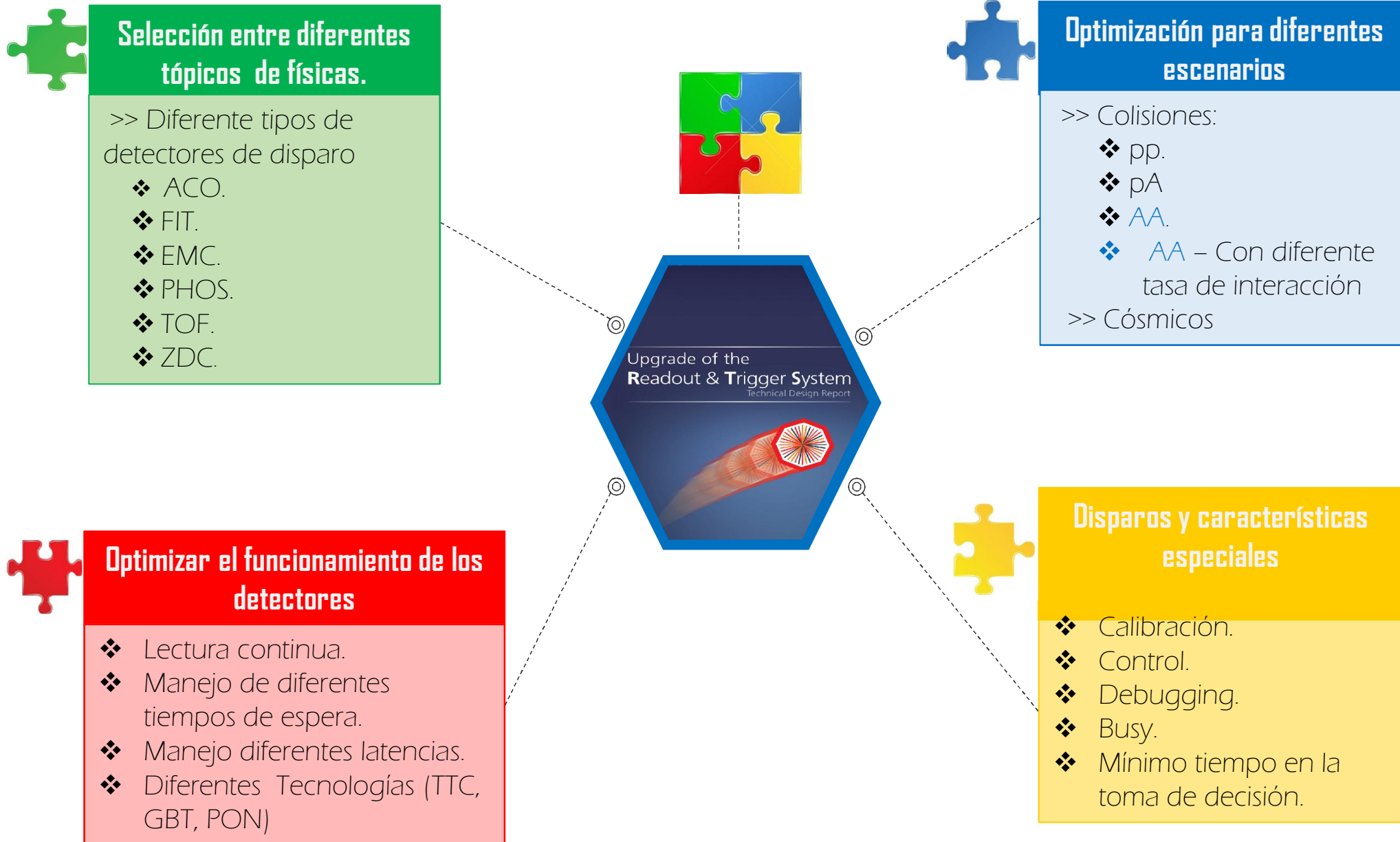
Luis Alberto Pérez Moreno – BUAP

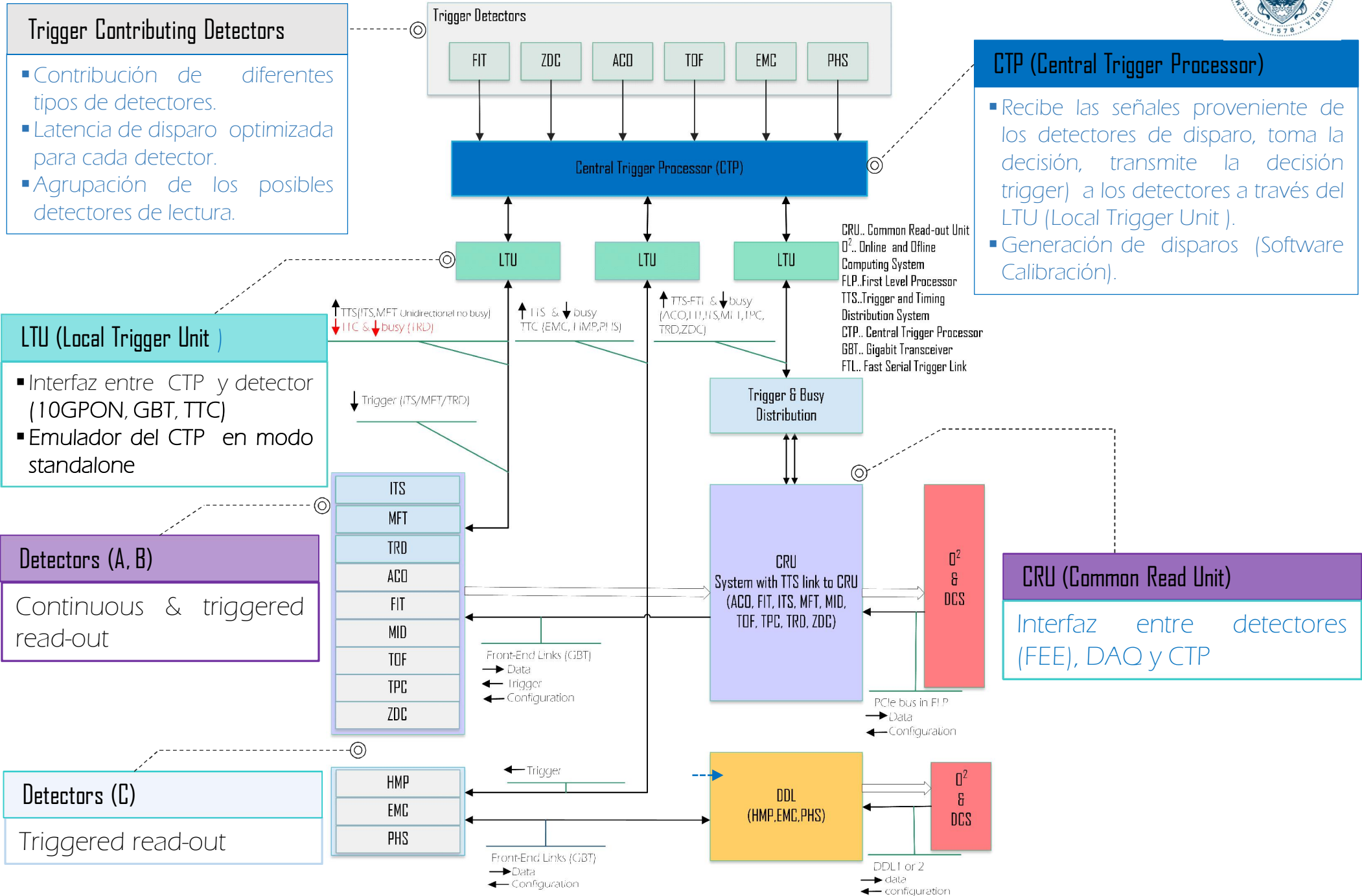
Outline

- ▶ CTP-Emulator (Data Frames)

CTP-Upgrade Meeting

25-April – 2016





**Trigger Contributing Detectors**

- Contribución de diferentes tipos de detectores.
- Latencia de disparo optimizada para cada detector.
- Agrupación de los posibles detectores de lectura.

**CTP (Central Trigger Processor)**

- Recibe las señales proveniente de los detectores de disparo, toma la decisión, transmite la decisión trigger) a los detectores a través del LTU (Local Trigger Unit).
- Generación de disparos (Software Calibración).

**LTU (Local Trigger Unit)**

- Interfaz entre CTP y detector (10GPON, GBT, TTC)
- Emulador del CTP en modo standalone

**Detectors (A, B)**

Continuous & triggered read-out

**Detectors (C)**

Triggered read-out

**CRU (Common Read Unit)**

Interfaz entre detectores (FEE), DAO y CTP



## Clasificación



### Detectores A (e.g. TPC, ACO, FIT)

- Detectores con FTL donde la latencia no es crítica,
- CRU = Distribución de trigger
- CRU = Readout

### Detectores B (e.g. ITS, MFT)

- Detectores con FTL donde la latencia es crítica,
- CTP = Distribución de trigger (GBT)
- CRU = Readout

### Detector C : ( Sin actualización)

- Detectores con FTL donde la latencia es crítica,
- CTP = Distribución de trigger (TTC)
- DDL = Readout

### TRD ( Caso Especial)

- CTP = Distribución de trigger (TTC)
- CRU = Readout

## Definición



### Trigger Type (Ttype) (16 bits)

1. Orbit
2. HeartBeat Accept
3. HeartBeat Reject
4. Prepulse
5. Calibration
6. Start of Continuous Data
7. Start of Trigger Data
8. End of Data

### Event ID (EVID) (44 bits)

- Contadores del CTP (Start LM Level)
- LHC BC (BCID): 12 bits
- Orbit Counter (ORBIT): 32 bits
- Standalone = Generados por el Emulador

### Trigger Input Mask (74 bits)

- Trigger inputs activated (TIM): 74 bits

### Detector Mask (18 bits)

- Detector included in the event (DM): 18 bits

### LM/L0/L1 time

- LM time: FIT input arrival at CTP.
- L0/L1 time: LM + delay, delay related to L0/L1 input

### Heart Beat Trigger (HB)

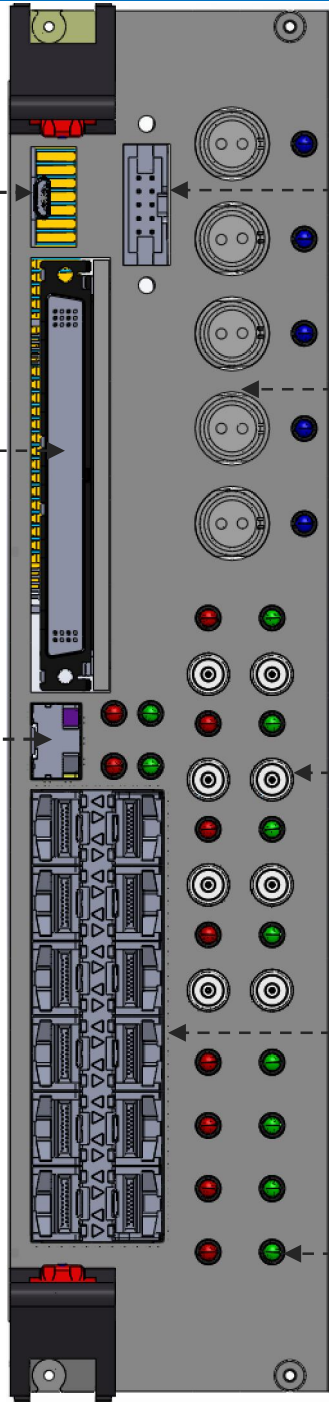
- Special Trigger type sent, every ~ 100  $\mu$ s to delimited data at CRU



- USB-JTAG(Programming of FPGA and SPI memory)

- FMC board (96 LVDS I/O Samtec)-Trigger inputs

- SFP + for IP bus (it must be separate as SFP for RJ45 has wider end if SFP plug-in module)



- PM bus connector (Voltage and temperatura monitoring)

- 5 x LVDS LEMO (2x LM/L0 out, BUSY in, BUSY out, Fast LM in)

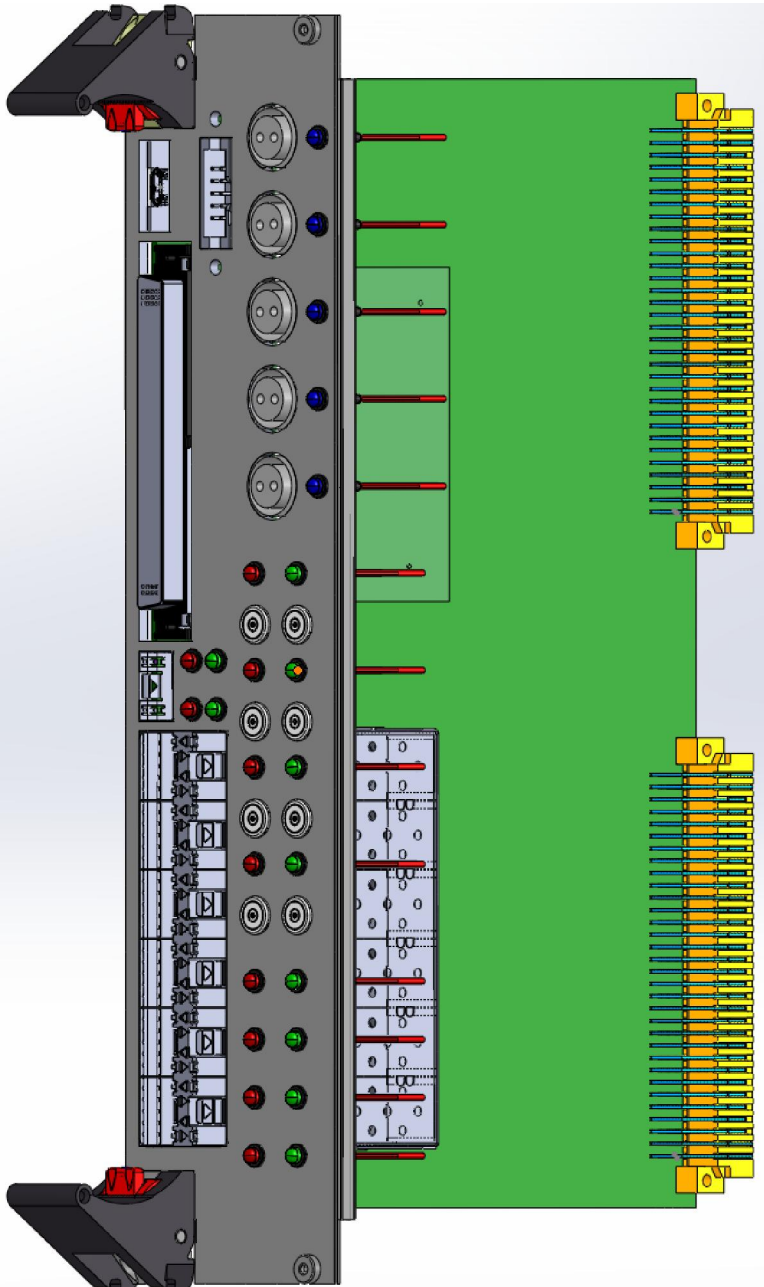
- 5 x Lemo 00 B (BC in, ORBIT in, Scope A out, Scope B out, TTC-A out, TTC-B out, Pulser in Spare in/out)

- 2x6 SFP +(12 x GBT or 10GPON)

- LEDs

**Diseño:**

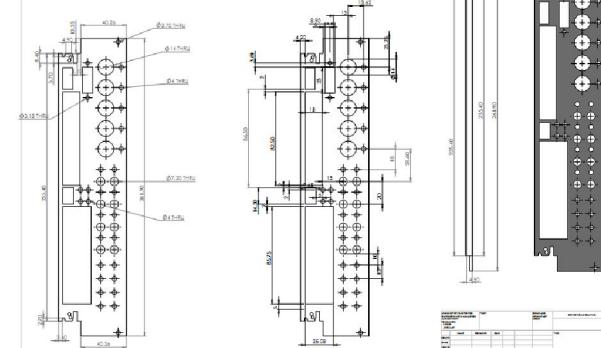
- Tarjeta VME 6U (Solo como Fuente de alimentación).
- PLL con fase fija IN/OUT (120/240 Mhz clock) (Silicon Labs 5338).



Trigger Board (Isométrica)

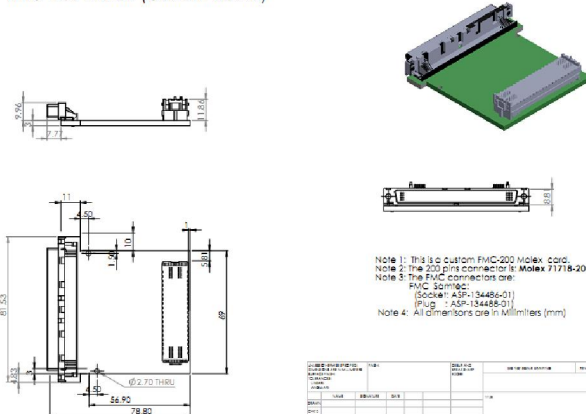
FRONT PANEL (ALICE TRIGGER BOARD)

NOTE 1: The base of this front panel is: EUMA 4U 12 HP (EUMA 66-22-24)  
NOTE 2: All dimensions in Millimetres (mm)



REV	DESCRIPTION	DATE	BY	CHK
1	Initial Release			

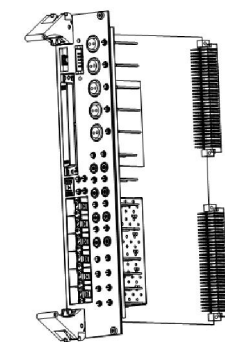
FMC-200 Molex (Custom board)



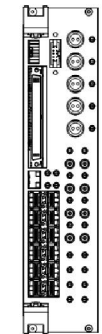
Note 1: This is a custom FMC-200 Molex card.  
Note 2: The 200 pins connector is: Molex 71718-2000  
Note 3: The FMC connectors are:  
FMC 32mm I/O  
(Socket: ASP-13448-01)  
(Plug: ASP-13448-01)  
Note 4: All dimensions are in Millimetres (mm)

REV	DESCRIPTION	DATE	BY	CHK
1	Initial Release			

ALICE TRIGGER BOARD



ALICE Trigger Board (Components)	
LEMO 8 for Chassis	LEMO 802.00.302.CLL
VME24x front Panel in 12HP	EUMA 66-22-24
FM Bus Connector	SKV 14-10
LEMO 8 for Chassis	LEMO 802.08.302.CLL
LEDs 3 mm panel Mount	Star PVA-COXY-2.0
Bottom Handle	EUMA 8-1265
Top Handle	EUMA 8-1265
USB-TAG module	Digitix PVA-D8V72
FMC Custom Card	Molex 71718-2000
SFP Cage	Molex 7444-1001
2x SFP Cage	TE connectivity 2007562-5
4x VME board	150 mm x 223 mm
VME connector	Standard



REV	DESCRIPTION	DATE	BY	CHK
1	Initial Release			



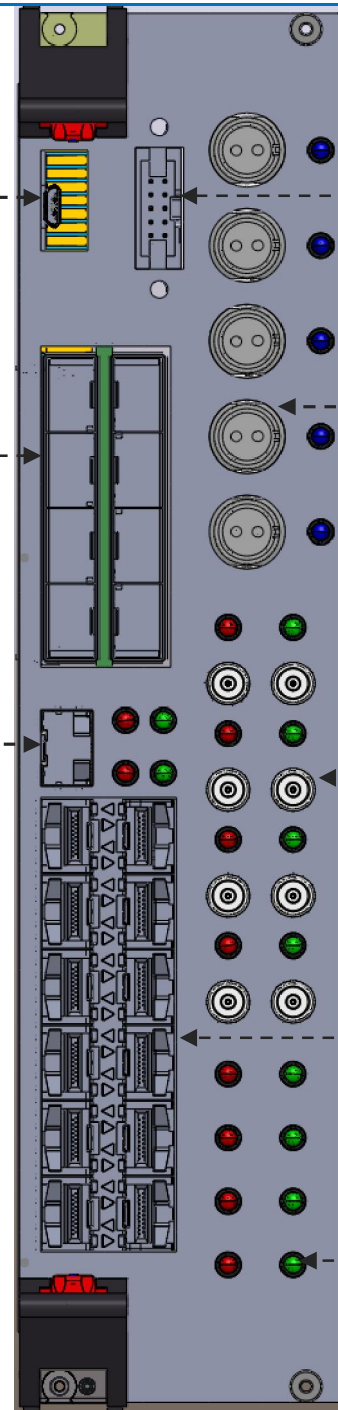
- USB-JTAG(Programming of FPGA and SPI memory)

- FMC board (Additional 8 SFP+ optical connectors) if required

- SFP + for IP bus (it must be separate as SFP for RJ45 has wider end if SFP plug-in module)

**Diseño:**

- Tarjeta VME 6U (Solo como Fuente de alimentación).
- PLL con fase fija IN/OUT (120/240 Mhz clock) (Silicon Labs 5338).



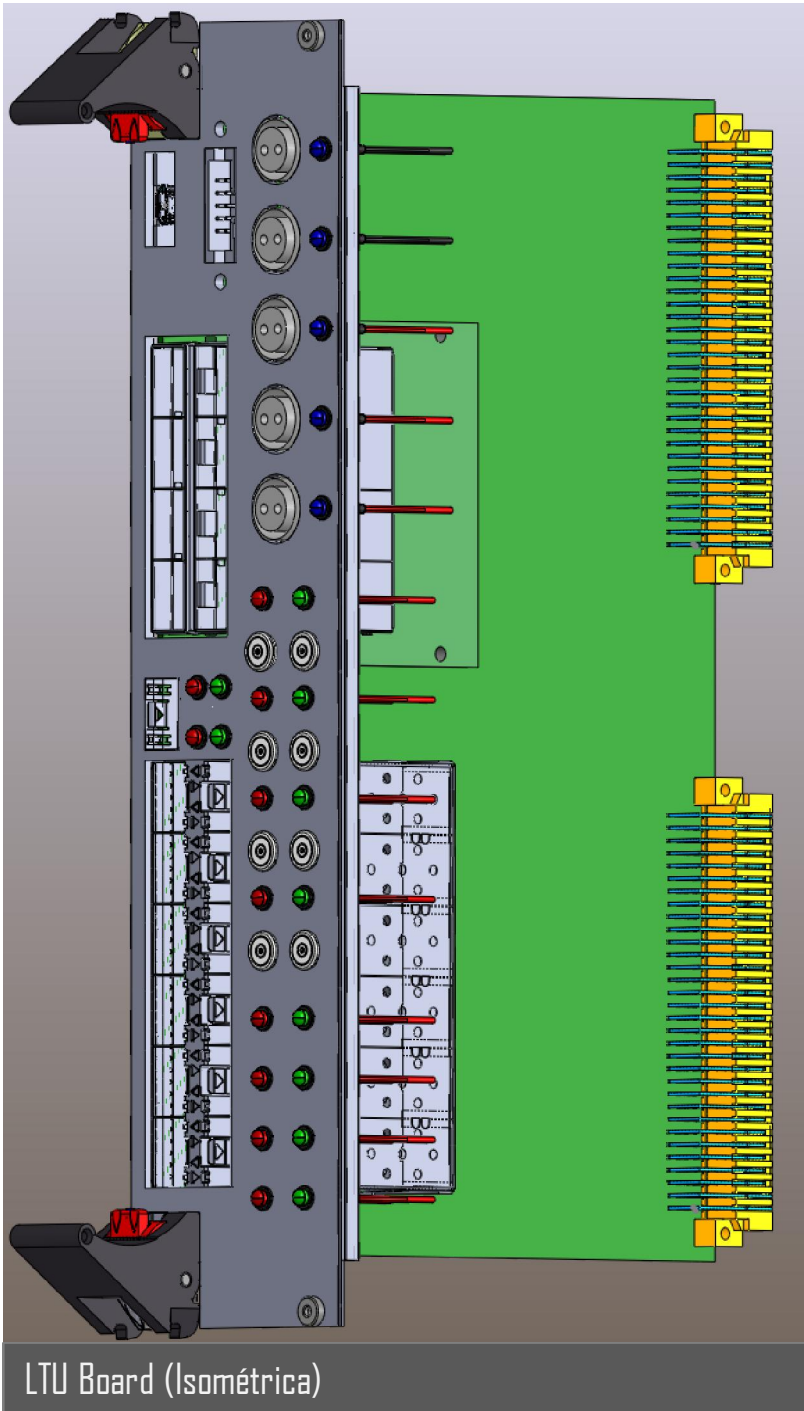
- PM bus connector (Voltage and temperatura monitoring)

- 5 x LVDS LEMO (2x LM/L0 out, BUSY in, BUSY out, Fast LM in)

- 5 x Lemo 00 B (BC in, ORBIT in, Scope A out, Scope B out, TTC-A out, TTC-B out, Pulser in Spare in/out)

- 2x6 SFP +(12 x GBT or 10GPON)

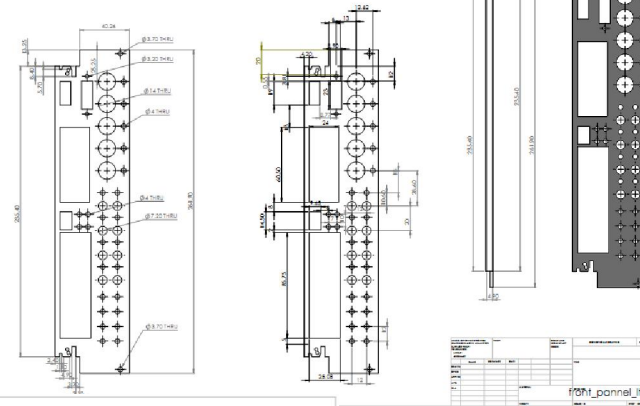
- LEDs



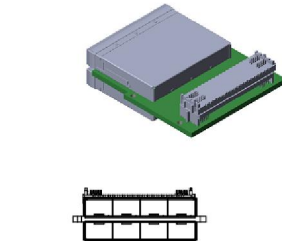
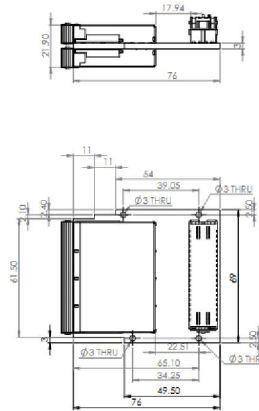
LTU Board (Isométrica)

## FRONT PANEL (ALICE LTU BOARD)

NOTE 1: The base of this front panel is: EUMA 6U 12 HP (EUMA 66-522-26)  
NOTE 2: All dimensions are millimeters (mm).



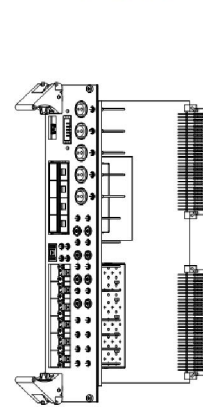
## FMC-SFP (FM-S18 Octal SFP/SFP+) (Faster Technology)



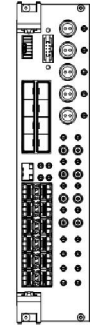
Note 1: The base of this FMC board is (VITA57) (Faster Technology)  
Note 2: The SFP cage is (Molex 1x4 SFP)  
Note 3: The FMC connectors are FMC Samtec:  
(Socket: ASP-134488-01)  
(Plug: ASP-134488-01)  
Note 4: All dimensions are in millimeters (mm)

NO.	DESCRIPCIÓN	TÍTULO	FECHA	PROYECTO	PROYECTANTE	REVISOR
1	...	...	...	...	...	...
2	...	...	...	...	...	...
3	...	...	...	...	...	...
4	...	...	...	...	...	...
5	...	...	...	...	...	...
6	...	...	...	...	...	...
7	...	...	...	...	...	...
8	...	...	...	...	...	...
9	...	...	...	...	...	...
10	...	...	...	...	...	...
11	...	...	...	...	...	...
12	...	...	...	...	...	...
13	...	...	...	...	...	...
14	...	...	...	...	...	...
15	...	...	...	...	...	...
16	...	...	...	...	...	...
17	...	...	...	...	...	...
18	...	...	...	...	...	...
19	...	...	...	...	...	...
20	...	...	...	...	...	...
21	...	...	...	...	...	...
22	...	...	...	...	...	...
23	...	...	...	...	...	...
24	...	...	...	...	...	...
25	...	...	...	...	...	...
26	...	...	...	...	...	...
27	...	...	...	...	...	...
28	...	...	...	...	...	...
29	...	...	...	...	...	...
30	...	...	...	...	...	...
31	...	...	...	...	...	...
32	...	...	...	...	...	...
33	...	...	...	...	...	...
34	...	...	...	...	...	...
35	...	...	...	...	...	...
36	...	...	...	...	...	...
37	...	...	...	...	...	...
38	...	...	...	...	...	...
39	...	...	...	...	...	...
40	...	...	...	...	...	...
41	...	...	...	...	...	...
42	...	...	...	...	...	...
43	...	...	...	...	...	...
44	...	...	...	...	...	...
45	...	...	...	...	...	...
46	...	...	...	...	...	...
47	...	...	...	...	...	...
48	...	...	...	...	...	...
49	...	...	...	...	...	...
50	...	...	...	...	...	...
51	...	...	...	...	...	...
52	...	...	...	...	...	...
53	...	...	...	...	...	...
54	...	...	...	...	...	...
55	...	...	...	...	...	...
56	...	...	...	...	...	...
57	...	...	...	...	...	...
58	...	...	...	...	...	...
59	...	...	...	...	...	...
60	...	...	...	...	...	...
61	...	...	...	...	...	...
62	...	...	...	...	...	...
63	...	...	...	...	...	...
64	...	...	...	...	...	...
65	...	...	...	...	...	...
66	...	...	...	...	...	...
67	...	...	...	...	...	...
68	...	...	...	...	...	...
69	...	...	...	...	...	...
70	...	...	...	...	...	...
71	...	...	...	...	...	...
72	...	...	...	...	...	...
73	...	...	...	...	...	...
74	...	...	...	...	...	...
75	...	...	...	...	...	...
76	...	...	...	...	...	...
77	...	...	...	...	...	...
78	...	...	...	...	...	...
79	...	...	...	...	...	...
80	...	...	...	...	...	...
81	...	...	...	...	...	...
82	...	...	...	...	...	...
83	...	...	...	...	...	...
84	...	...	...	...	...	...
85	...	...	...	...	...	...
86	...	...	...	...	...	...
87	...	...	...	...	...	...
88	...	...	...	...	...	...
89	...	...	...	...	...	...
90	...	...	...	...	...	...
91	...	...	...	...	...	...
92	...	...	...	...	...	...
93	...	...	...	...	...	...
94	...	...	...	...	...	...
95	...	...	...	...	...	...
96	...	...	...	...	...	...
97	...	...	...	...	...	...
98	...	...	...	...	...	...
99	...	...	...	...	...	...
100	...	...	...	...	...	...

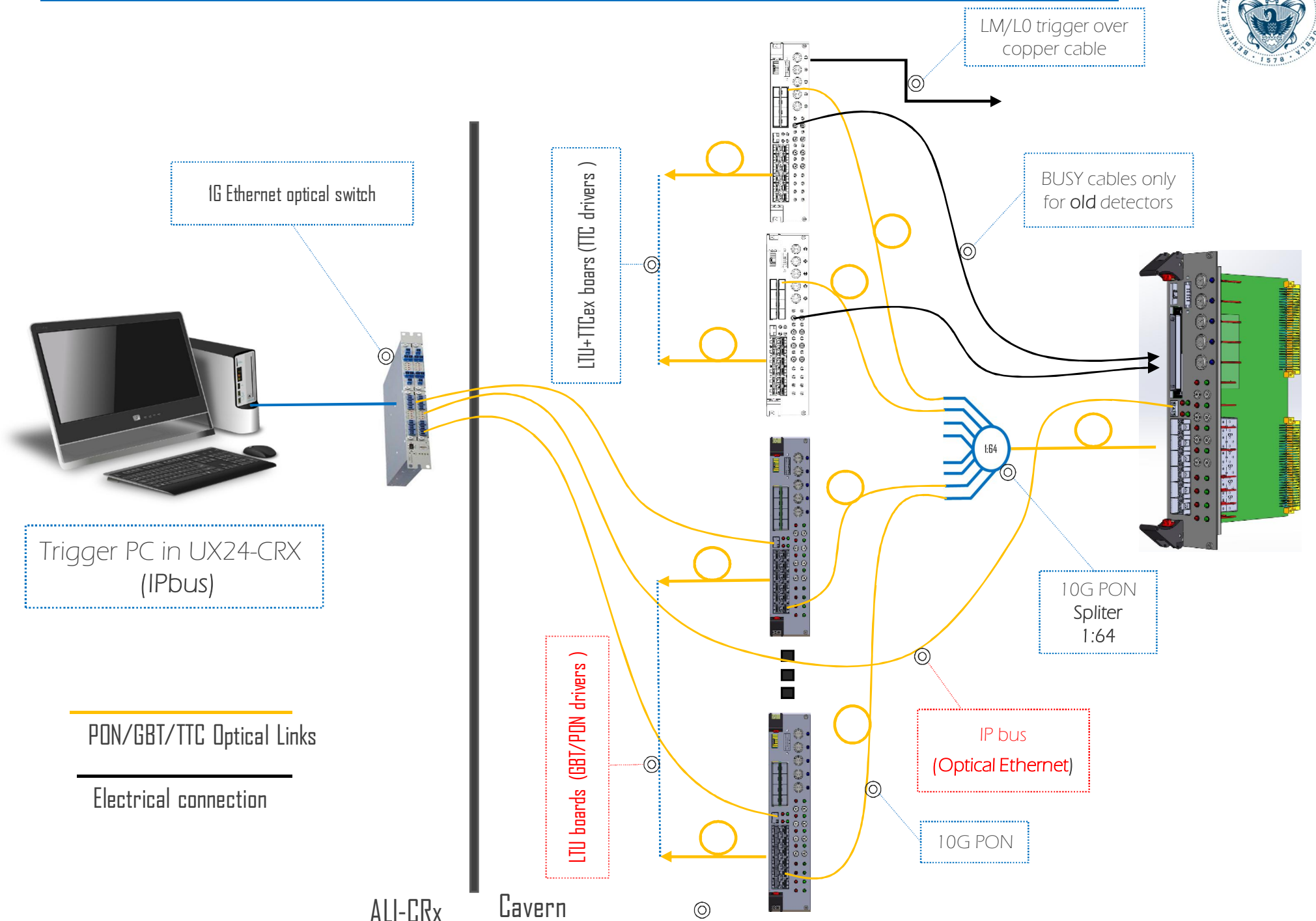
## ALICE LTU BOARD

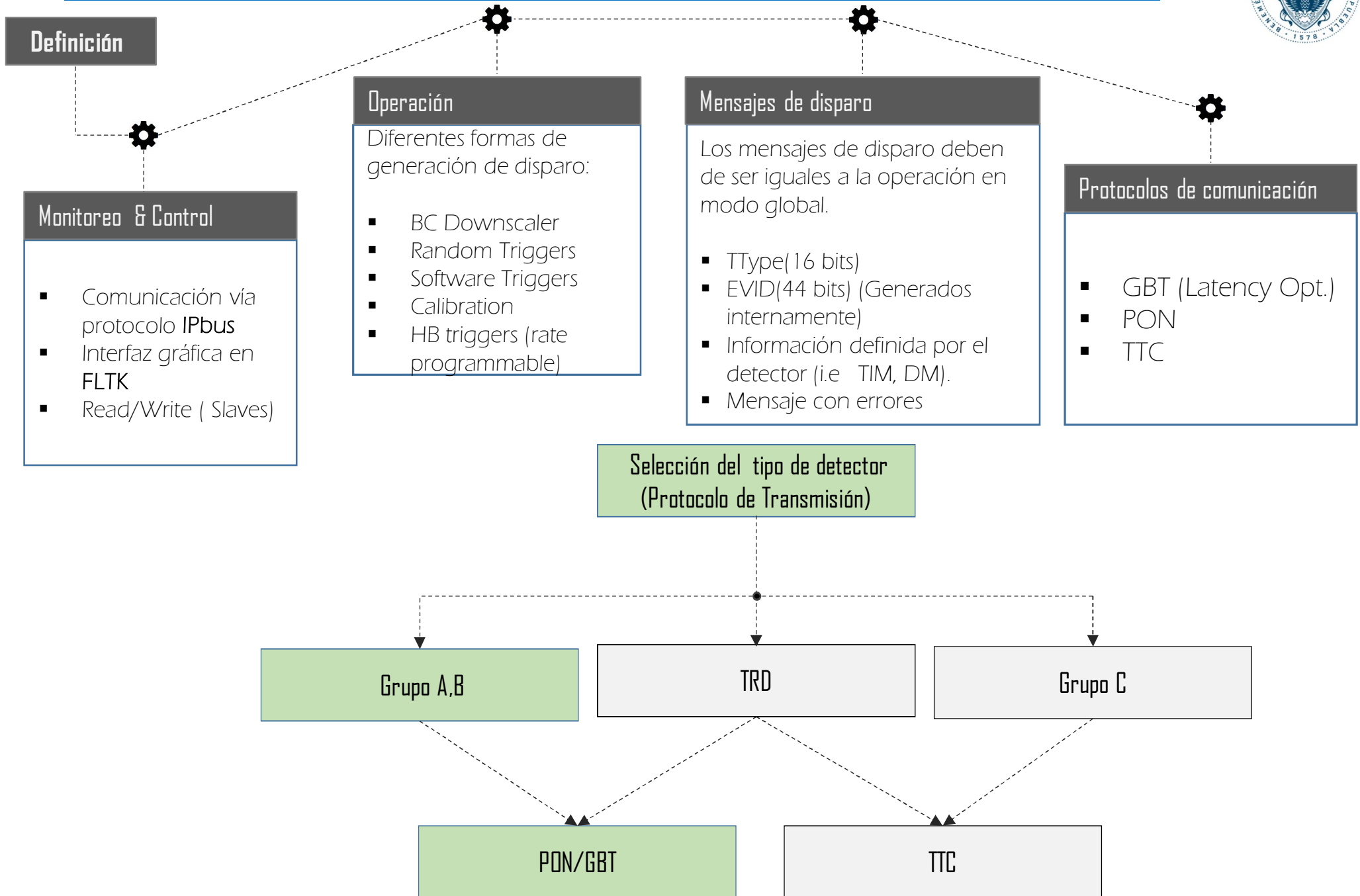


ALICE LTU Board (Component)	
LEMIO 008 for Chassis	LEMIO 008 00 803 011
VMElike Front Panel 6u 12HP	EUMA 66-522-26
FM Bus Connector	3U 4x10 (Plug)
LEMIO 8 for Chassis	LEMIO 008 00 803 011
LEDS 3 mm panel Mount	3mm PVB200V 12D
Bottom Handle	EUMA 81-026
Top Handle	EUMA 81-026
USB-JTAG module	Digitart JTAG-SMT2
FMC-SFP Card	FMS18 008 SFP/SFP+ transceiver FMC
SFP Cage	Molex 7444-0001
3u SFP Cage	TE connectivity 20975626
6u VME board	1160 mm x 233 mm
VME connector	Standard





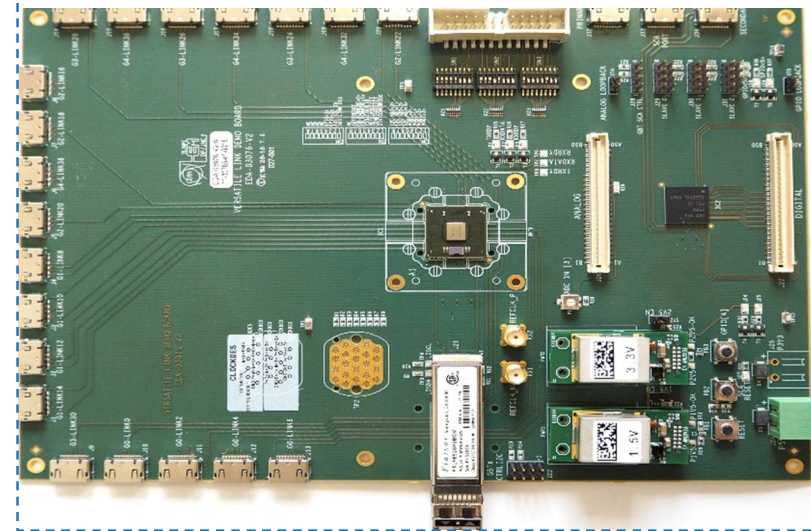






▶ Trigger PC

▶ Versatil Link Demo Board (GBTx)



1



Ethernet  
(Copper cable)

3



Optical Link

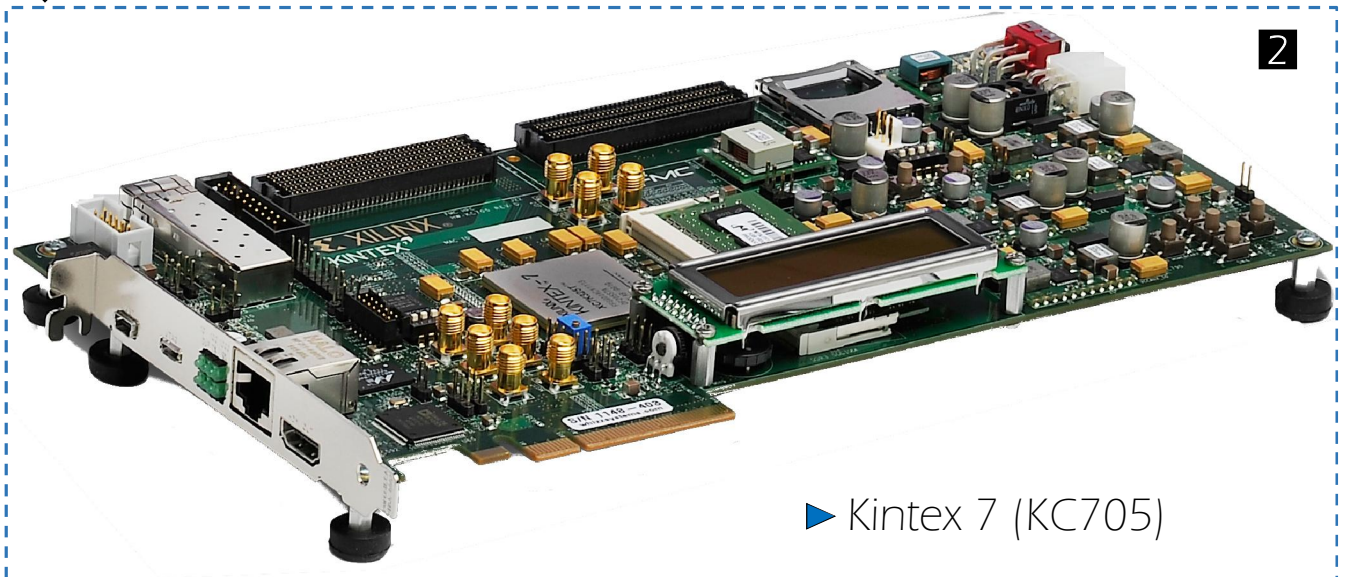
▶ Advanced goals :

- 1 IPbus control for CTP emulator
- 3 CTP emulator – GBT
- 2 Ipbus- CTP-Emulator-GBT- VLDB

▶ Note:

Because a commercial SFP is used, the polarity of the FPGA-GBT TX was “inverted”

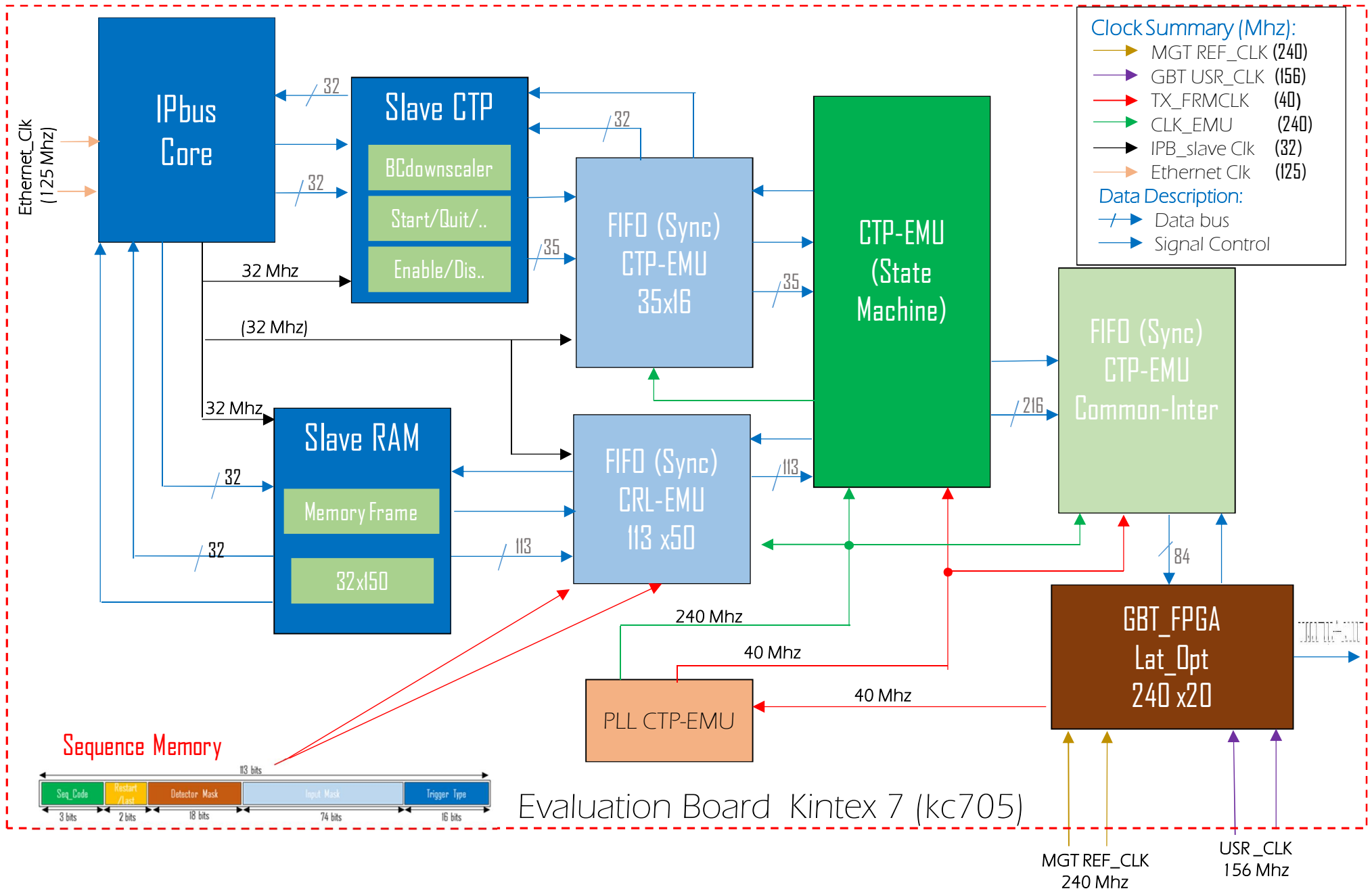
2



▶ Kintex 7 (KC705)



## Block Diagram (Clock Domain)

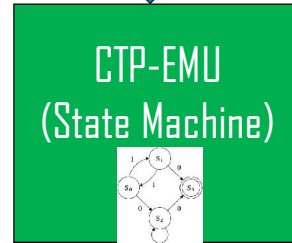
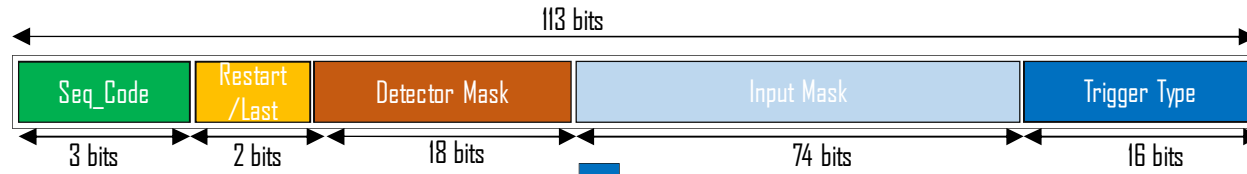




## Emulator Memory Frame

(Ref: Trigger System Design Review April 2016)

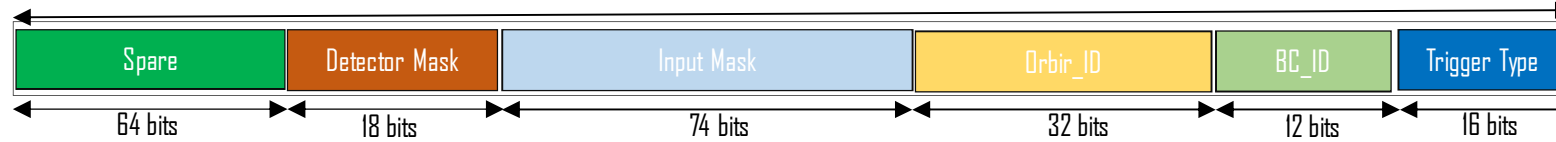
Seq_Code	Sequence Name	Sequence Structure	Sequence code
	LO	LO	1 ★
	LM	LM-LO	2
	Calibration Prepulse	PP	3
	Calibration LO	PP-LO	4
	Calibration LM	PP-LM-LO	5
Flow control in the CTP-Emulator			



- ### Trigger Type
1. Orbit
  2. HeartBeat Accept
  3. HeartBeat Reject
  4. Prepulse
  5. Calibration
  6. Start of Continuous Data
  7. Start of Trigger Data
  8. End of Data

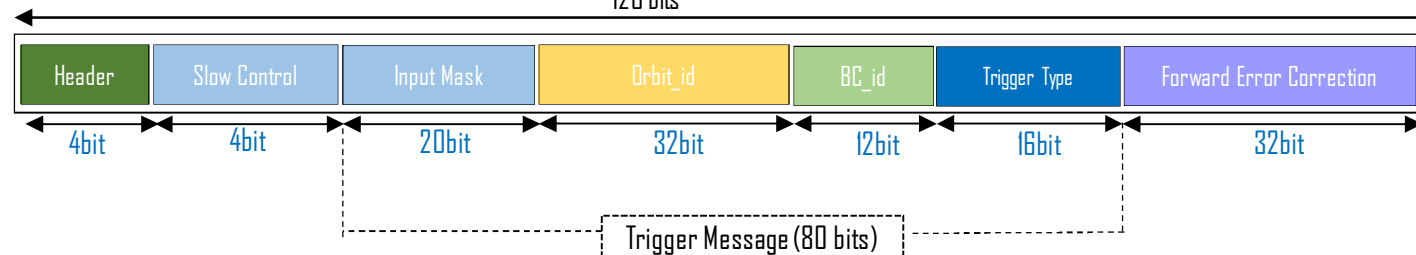
216 bits

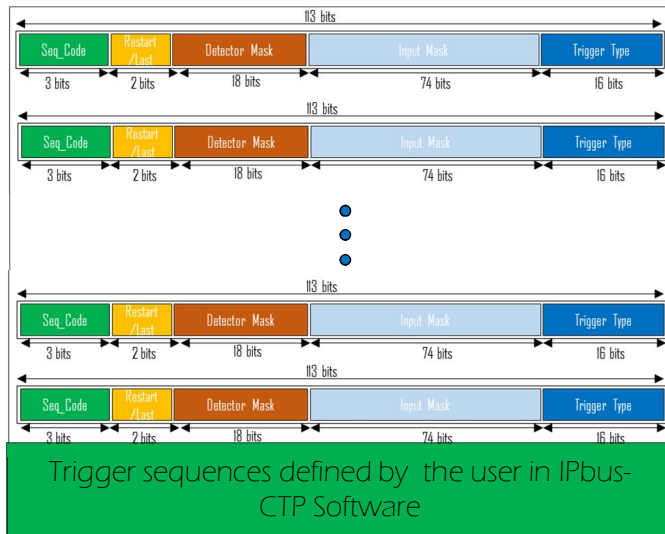
## CTP-Emulator Frame



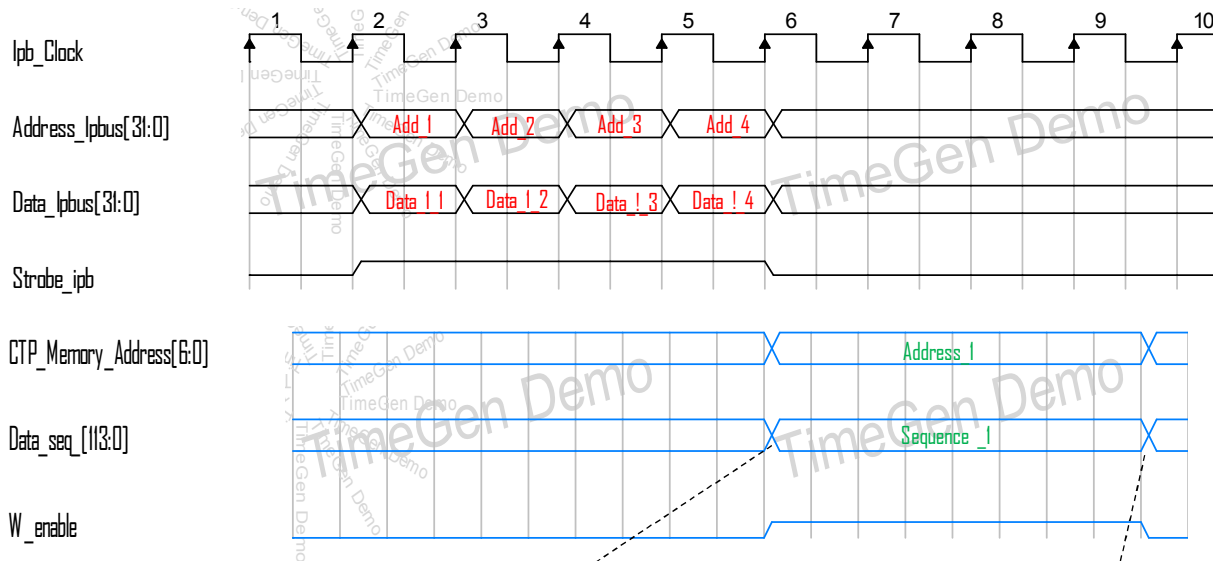
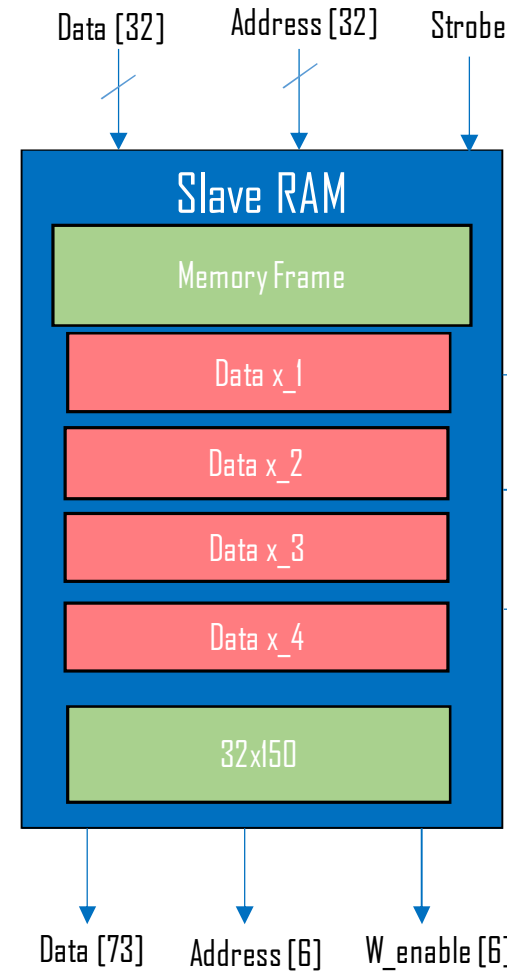
120 bits

## GBTFrame



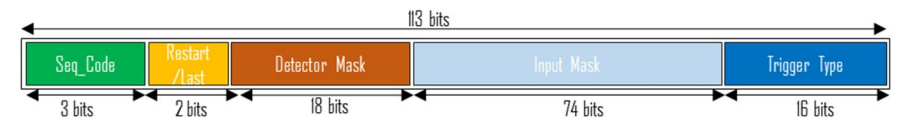


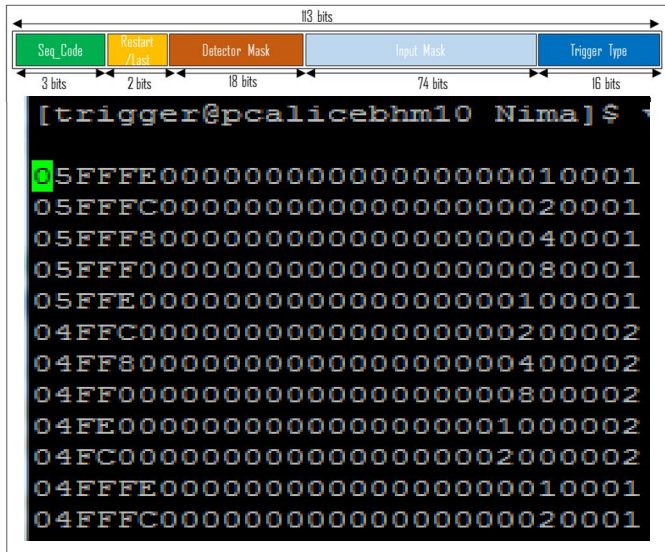
CTP/IPbus Software



Sequence 1 = Concatenate (Data\_1\_1 & Data\_1\_2 & Data\_1\_3 & Data\_1\_4)

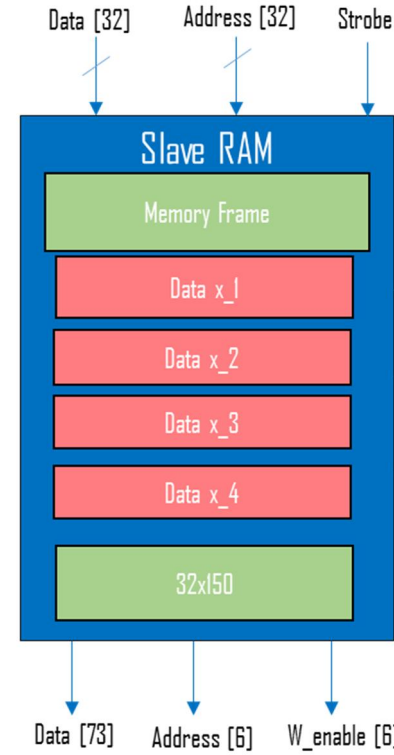
Sequence Memory



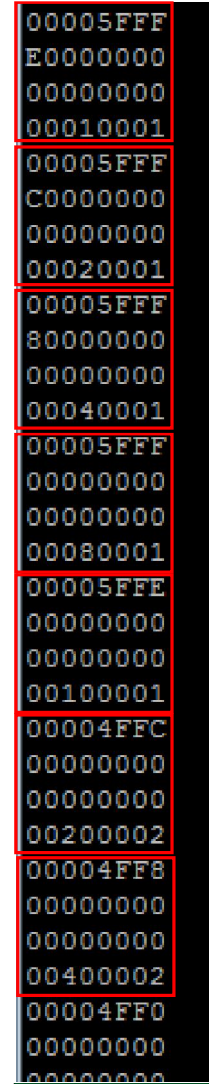


Trigger sequences defined by the user in IPbus-CTP Software

CTP/Ipb Software



Ipbus\_Rd



Trigger-PC

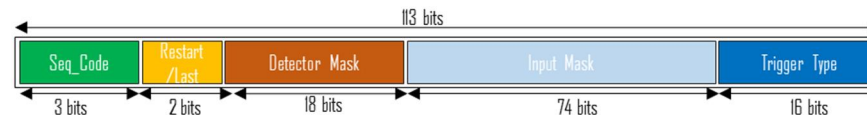
```
[trigger@pcalicebhm10 bin]$ ltuipbus
Which Register do you want?
ram
```

```
Would you like to input values (i) or read from txt file (r)
r
How many values do you wish to write
120
At what offset do you wish to start writing
0
Size vector: 120
```

Configuration in Trigger-PC

Sequence Memory

Sequence 1 = Concatenate (Data 1 | 8 Data 2 | 8 Data 3 | 8 Data 4)



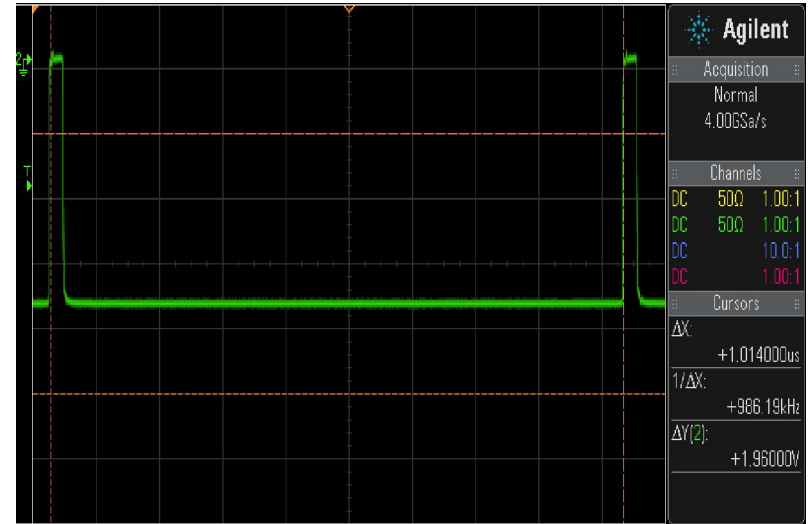


```

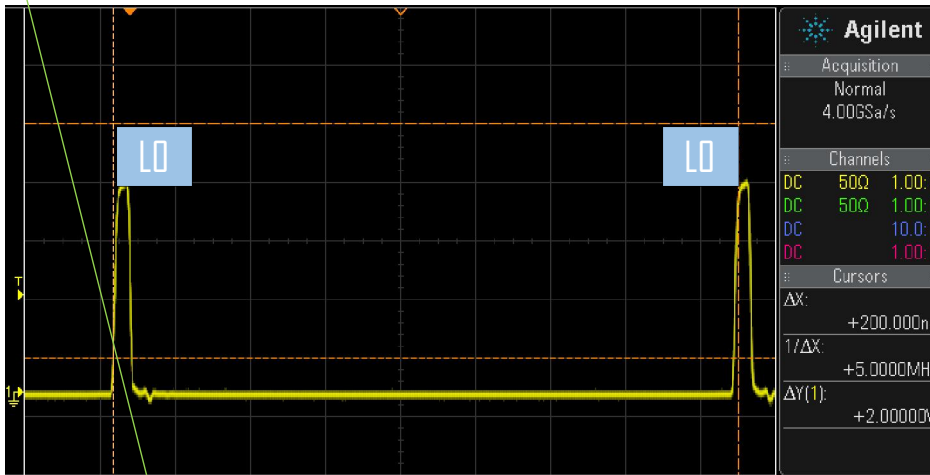
trigger@pcalicebhm10:~/ipbus/Nima/bin
/ipbus/Nima/bin/../../../../boards/ltu_kc705.xml"
+ Node "ram", INCREMENTAL block, Size 1024, Addresses [0x00001400-000017FF],
Permissions rw, Description "1kword emulation memory", Module "/home/alice/trig
ger/ipbus/Nima/bin/../../../../boards/ltu_kc705.xml"
29-02-16 09:41:38.967469 [7fbe47c4d720] INFO - URI "chtcp-2.0://localhost:10203?
target=137.138.140.146:50001" parsed as:
> protocol : chtcp-2.0
> hostname : localhost
> port : 10203
> path :
> extension :
> arguments :
> target = 137.138.140.146:50001

29-02-16 09:41:38.967538 [7fbe47c4d720] INFO - Converted IP address string "137.
138.140.146:50001" to 137.138.140.146:50001 and converted this to IP 0x898A8C92,
port 0xC351
Do you wish to Read (r) or Write (w)? or Write and Read (rw)?
r
29-02-16 09:41:40.508289 [7fbe47c4d720] INFO - Attempting to create TCP connecti
on to 'localhost' port 10203.
29-02-16 09:41:40.508966 [7fbe47c4d720] INFO - TCP connection succeeded
8
trigger@pcalicebhm10 bin]$
    
```

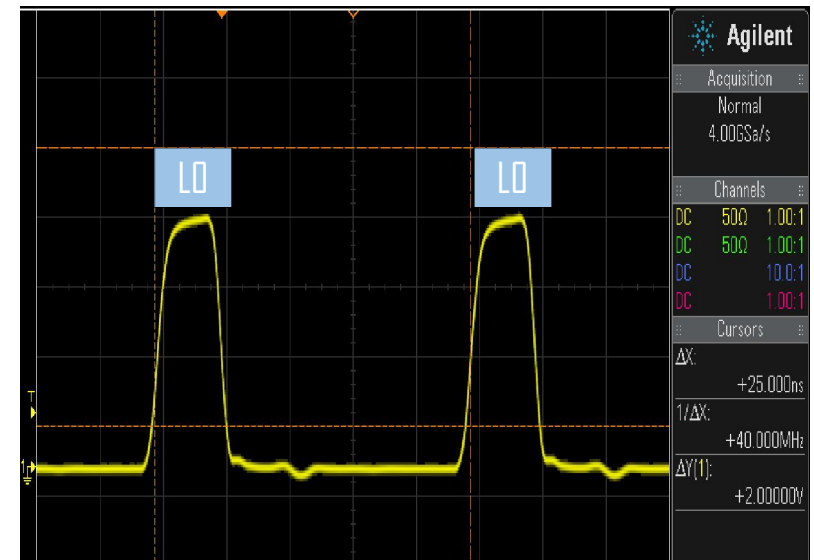
Control → (OK)



Test signal, Fixed to 1 us.



Bcrate = 8 BC ( 200 ns ) (LO - LO)



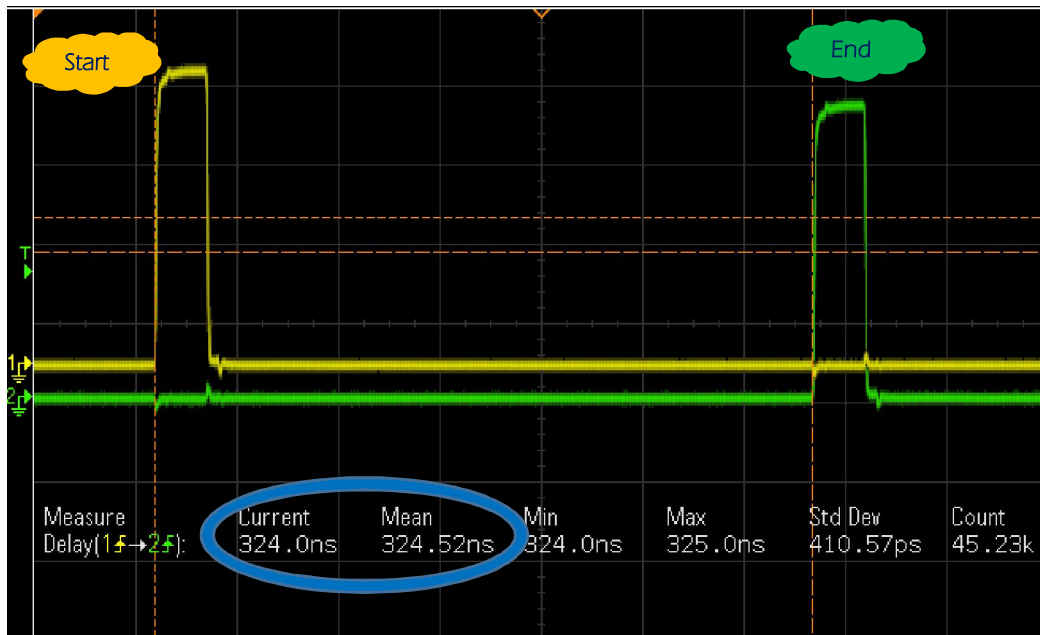
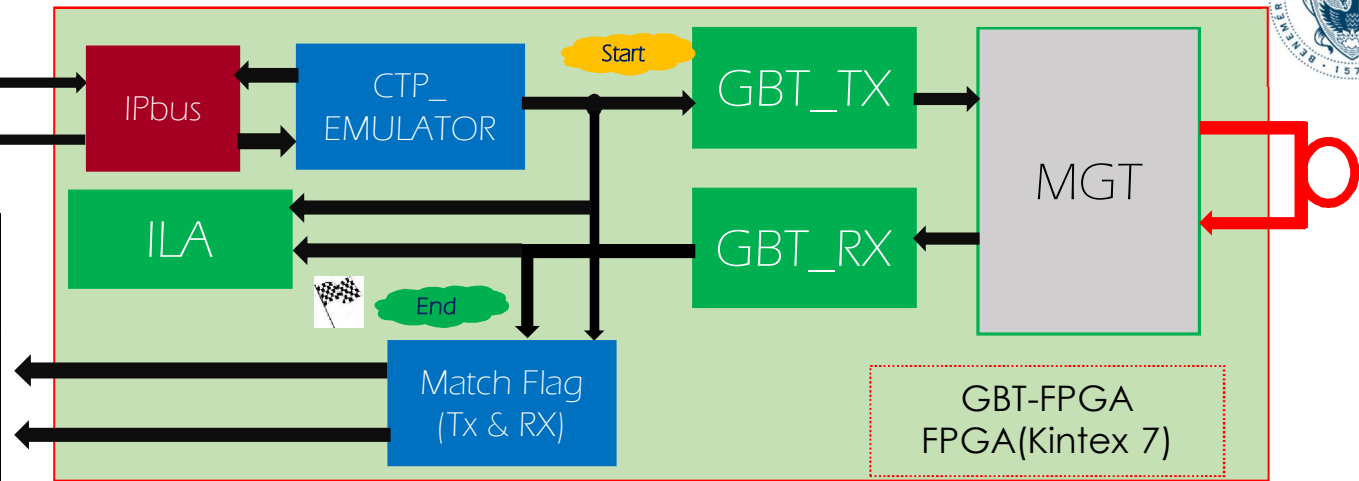
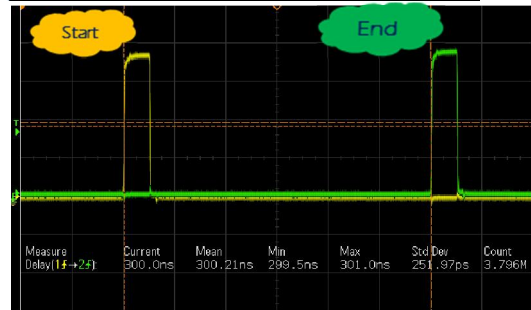
Bcrate = 1 BC ( 25 ns ) (LO - LO)



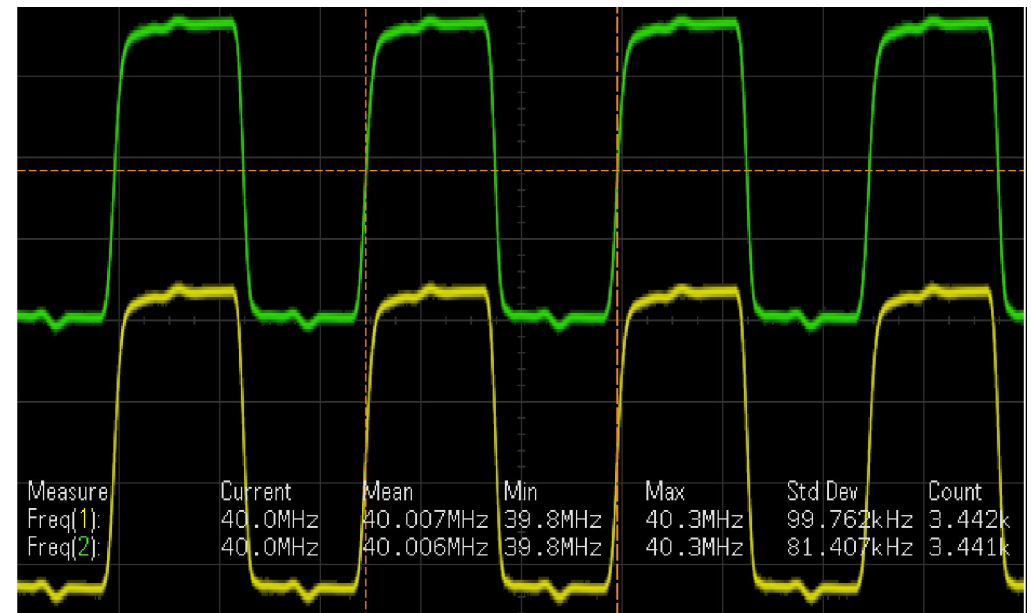
# Resultados (IPbus- CTP-Emulador – GBT )



```
[trigger@pcalicebhm10 bin]$ ltuipbus
Which Register do you want?
bcrate
Would you like to input values (i) or read from txt file (r)?
i
Do you wish to Read (r) or Write (w) or Write and Read (rw) or txt?
w
What value do you wish to write?
6
```



Time between (Match Flags TX & RX) ~ 324 ns (loopback)



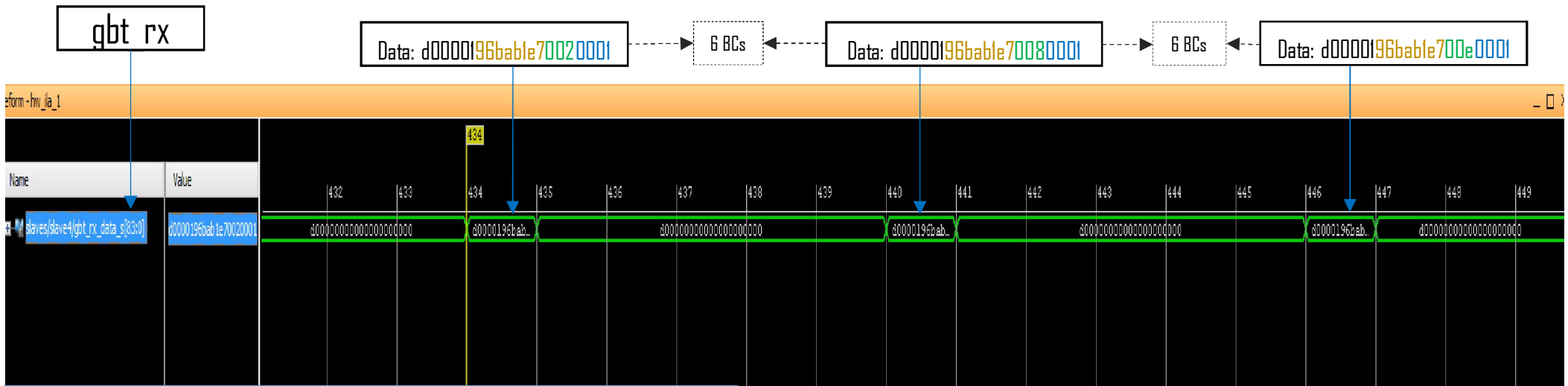
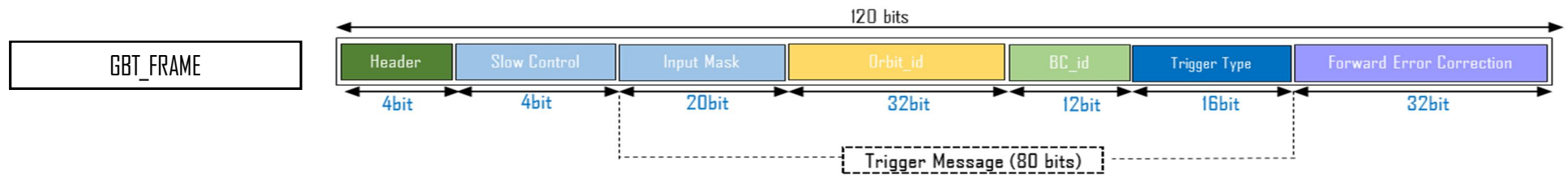
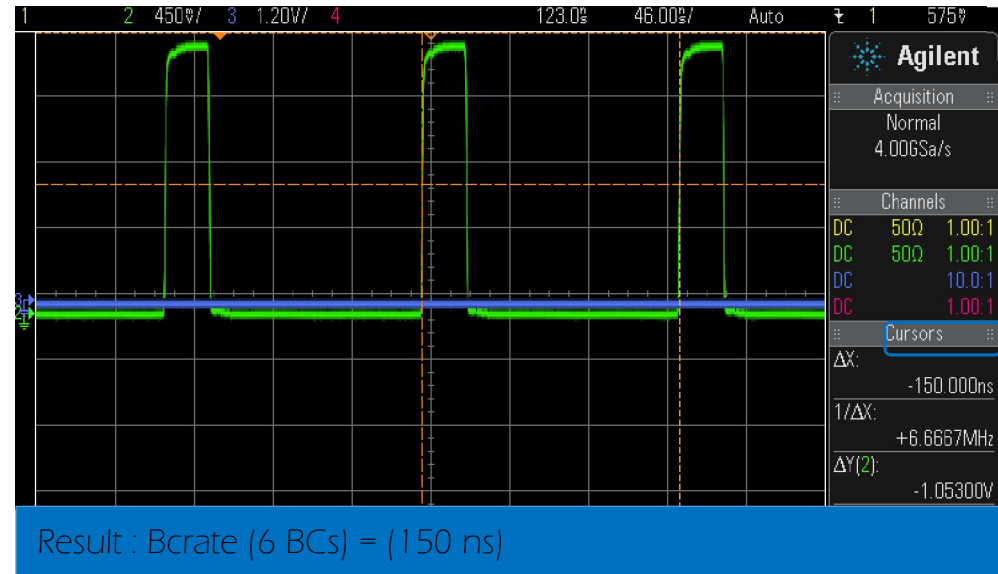
Phase relationship between (TX\_Frame\_clk & RX\_Frame\_clk)

- Rx\_Frame\_clk (40 Mhz.)
- TX\_Frame\_Clk (40 Mhz)

# Resultados (Mensajes de trigger)



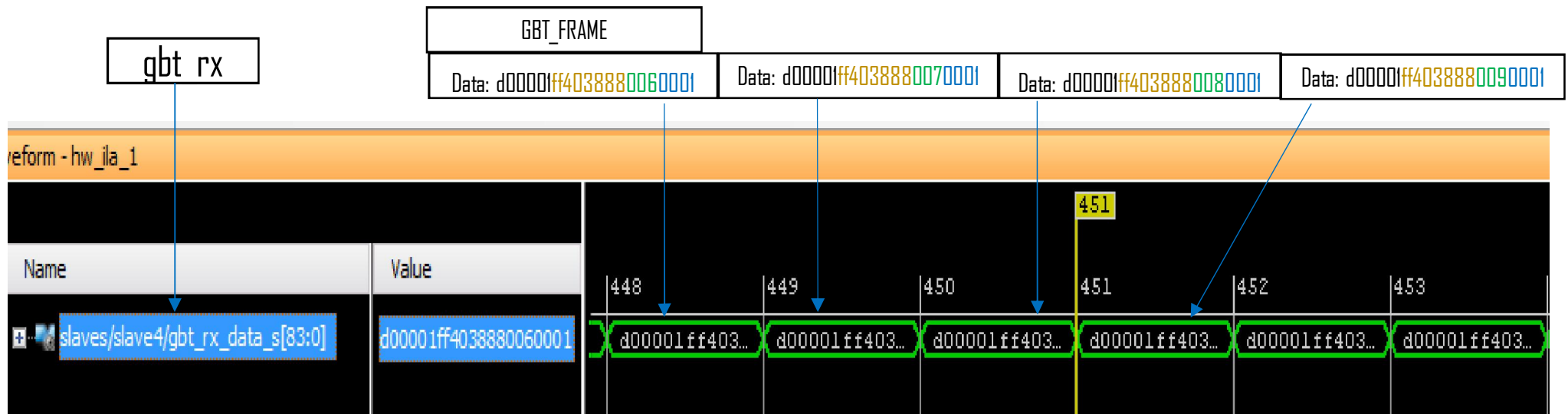
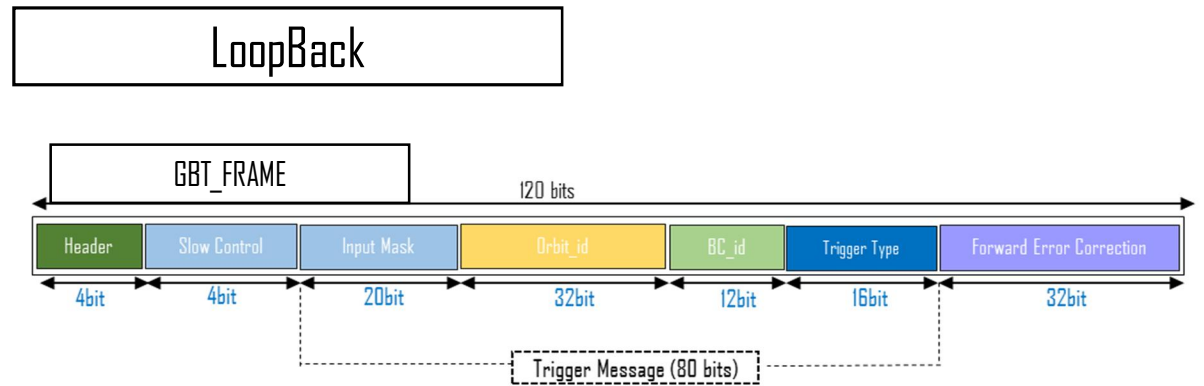
```
[trigger@pcalicebhm10 bin]$ ltuipbus
Which Register do you want?
bcrate
Would you like to input values (i) or read from txt file (t)
i
Do you wish to Read (r) or Write (w)? or Write and Read (rw) or txt?
w
What value do you wish to write?
6
Comunicación → (OK) Bcrate (6 BCs) = (150 ns)
```



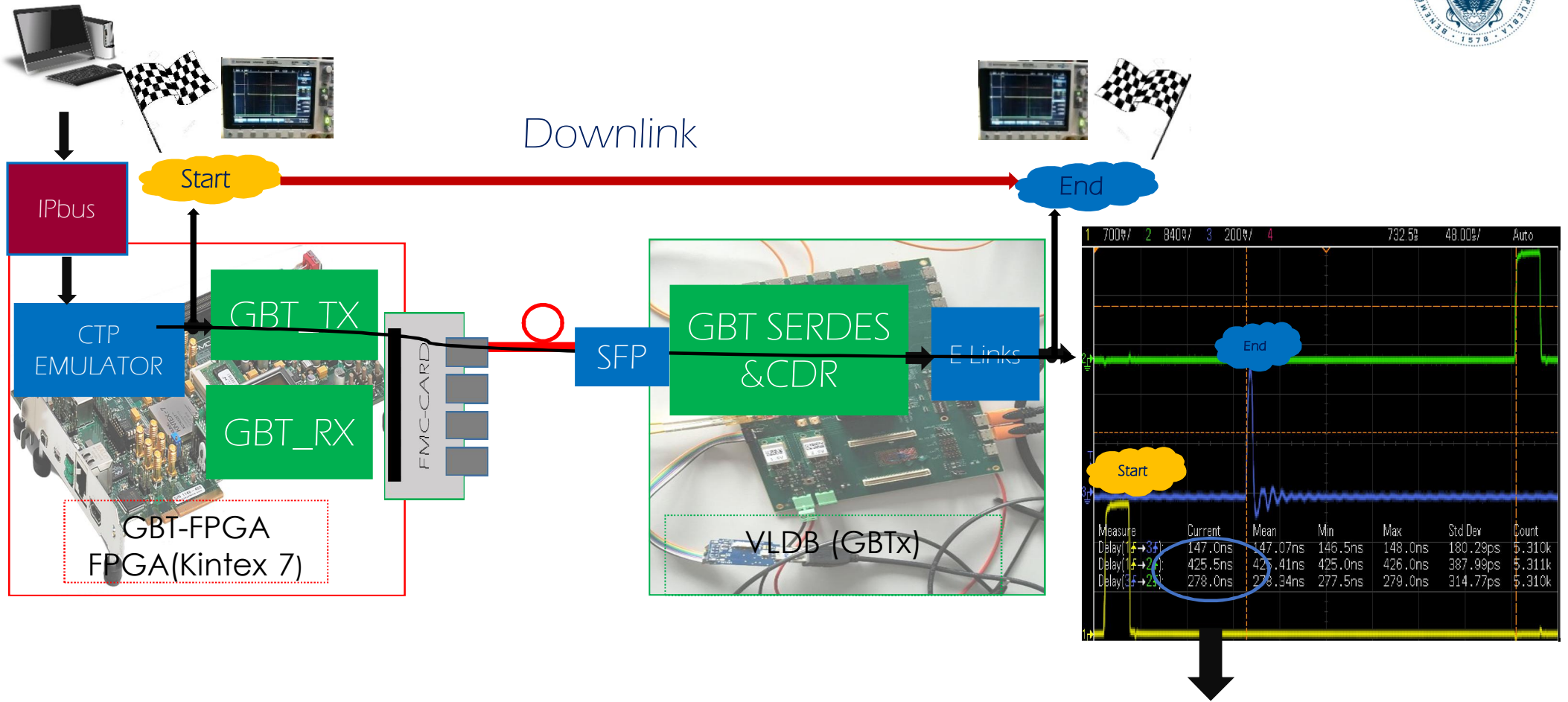
Trigger Message → OK

# Resultados (Mensajes de trigger (Rate\_Max ))

```
[trigger@pcalicebhm10 bin]$ ltuipbus
Which Register do you want?
bcrate
Would you like to input values (i) or read from txt file (t)
i
Do you wish to Read (r) or Write (w)? or Write and Read (rw) or txt?
w
What value do you wish to write?
1
Comunicacion -> (OK) Bcrate (1 BCs) = (25 ns)
```



Máximo (Rate) 40 MHz



▶ FPGA- Configuration

- FPGA → Kintex 7 (KC705)
- Software → VIVADO 2015.5
- GBT-FPGA → LAT\_OPT
- GBT\_ENCODER → GBT-FRAME
- FPGA -GTX → 240 Mhz -20 bits

▶ VLDB (GBTx) Configuration

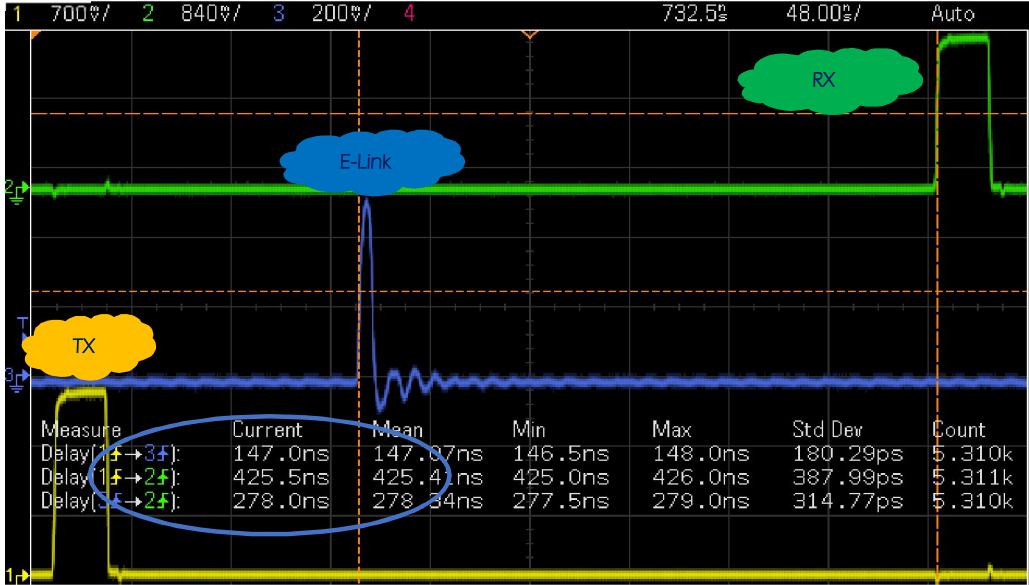
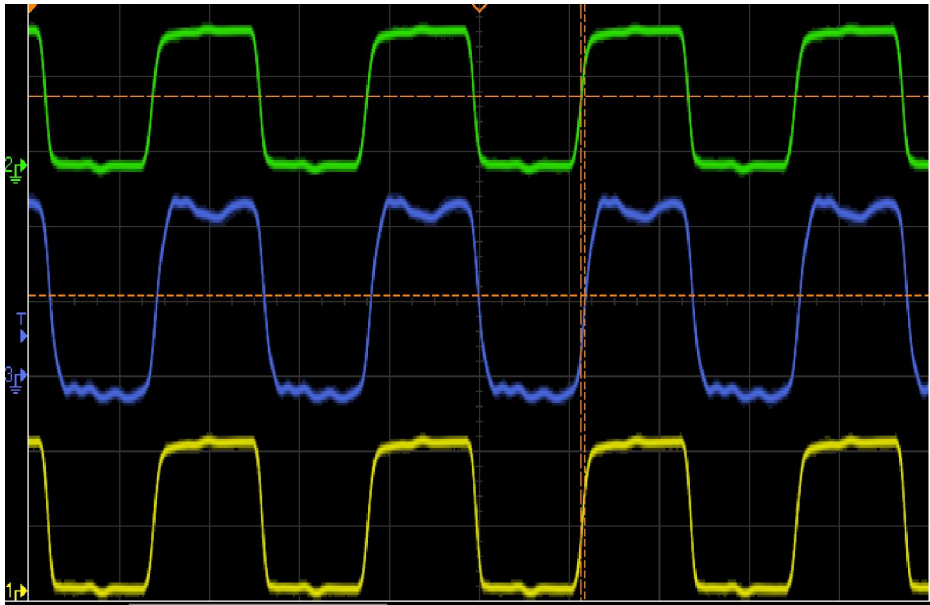
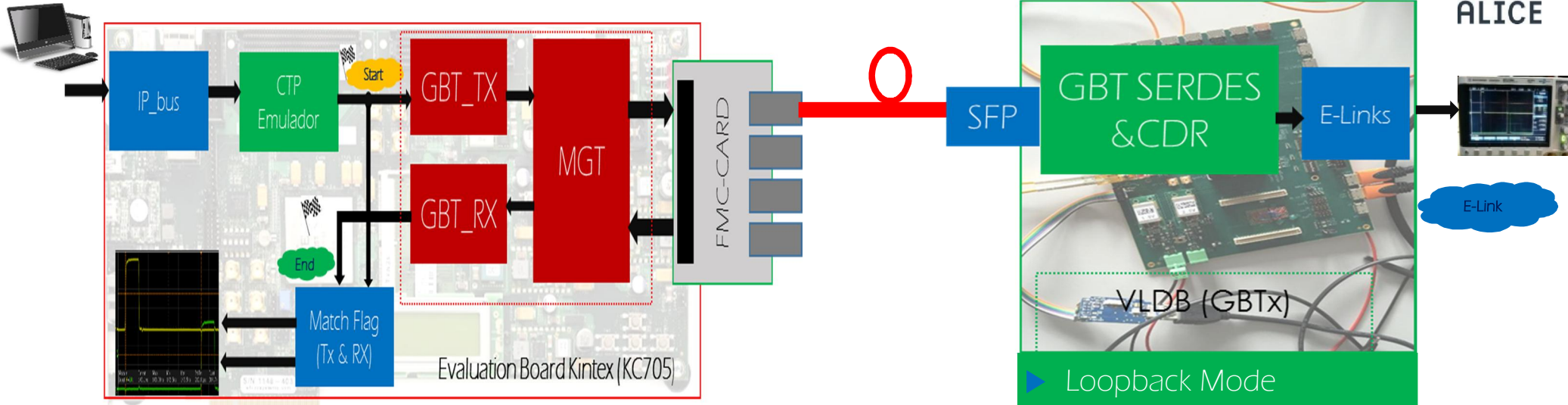
- DCDC → (3.3V) for SFP
- Clk\_Source → (internal xpll)
- Encoding → GBT TRX
- Phase Shifter → No
- Eport RX (dIn) → OFF
- EportTX (dOut) → 160 Mbits/S (G0, G1, G2)
- EportTX (dCLK) → 40 Mhz

▶ Summary Measurement

- Downstream Latency ~ 147 ns → 5 BCs
- Downstream - Cables ~ 140 ns → 5 BCs

# Setup (GBT/IP/ CTP Emulation) (Status)

A Large Ion Collider Experiment



## Clock Recovery

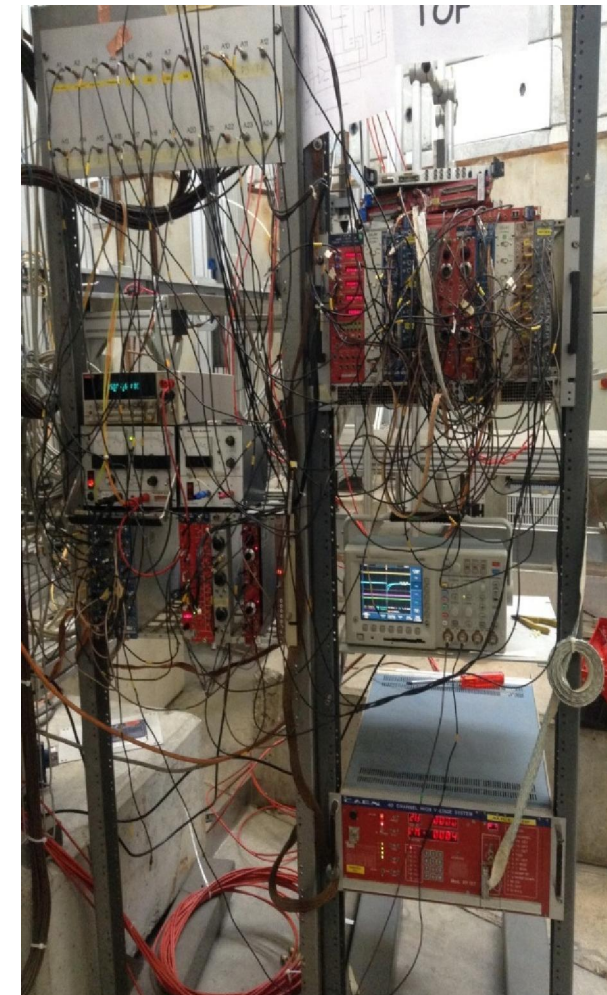
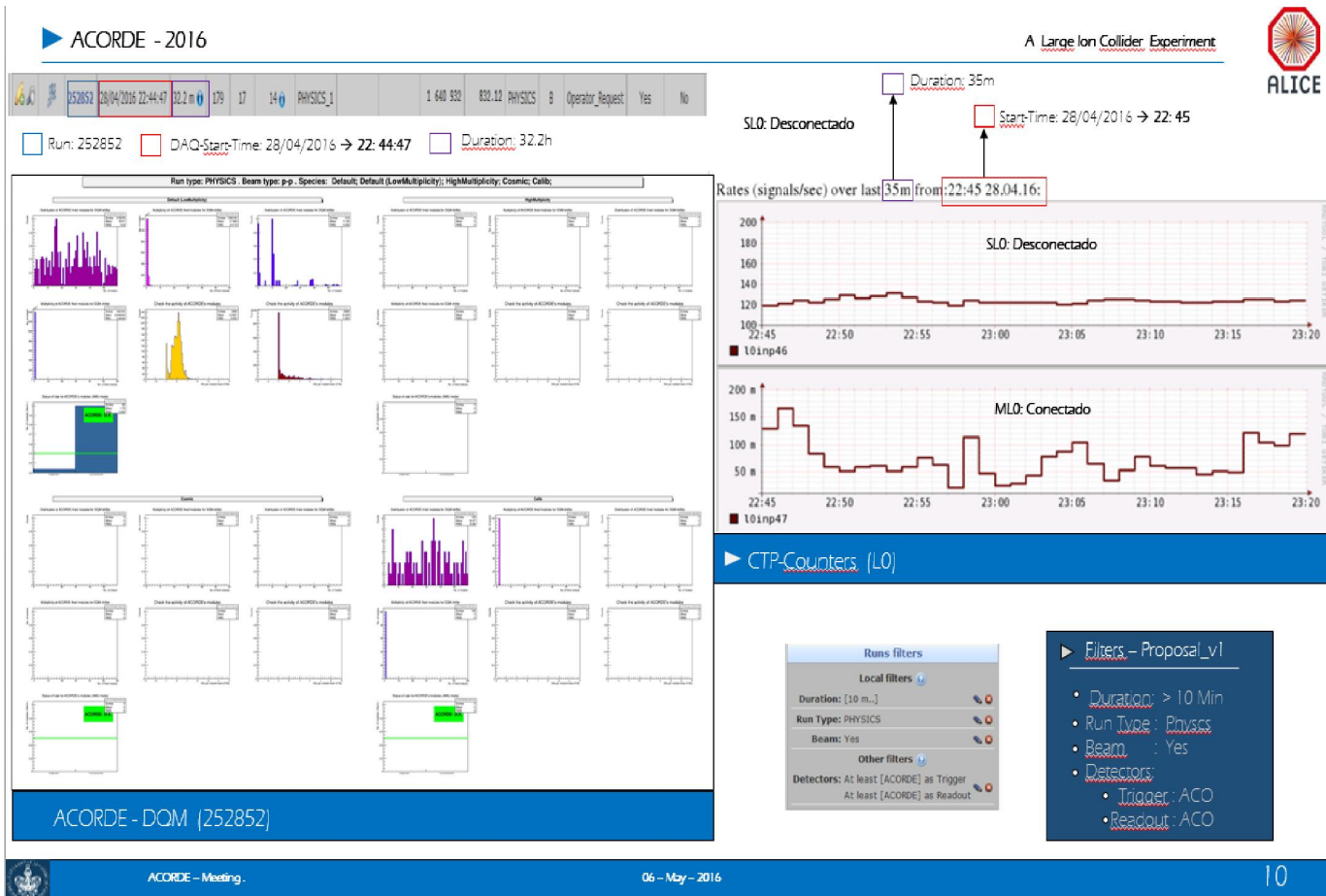
- CTP – GBT Transmitter 40 Mhz
- VLDB (GBTx) 40 Mhz
- CTP – GBT Receiver 40 Mhz

## Summary Measurement

- CTP-to-VLDB Downlink ~ 140 ns
- CTP – to – VLDB Loopback ~ 240 ns



- Monitorear el correcto funcionamiento del detector ACORDE
- Participar en el beam-test del detector ACORDE
- Creación de RPM para configuración de ACORDE



- Instalación ACORDE Beam-Test

- ACORDE Participando el periodo LHC RUN-2



## Resultados

- ALICE Trigger – TDR (Ver\_1)
- Diseño de LTU-b y CTP-b
- Version 1 CTP-Emulador (Bajo prueba por del detector TOF)
  - ❖ Interfaz IPbus (control y monitoreo)
  - ❖ Emulador (CTP standalone)
  - ❖ GBT (Latencia Óptima)
- Revisión de los posibles análisis físicos con la información generada por CTP



## Trabajo Futuro

- Pruebas con el LTU-b
- Verificar la transmisión por 10G PON
- Iniciar con el análisis físico









Gracias por su atención

E-mail: lperezmo@cern.ch.





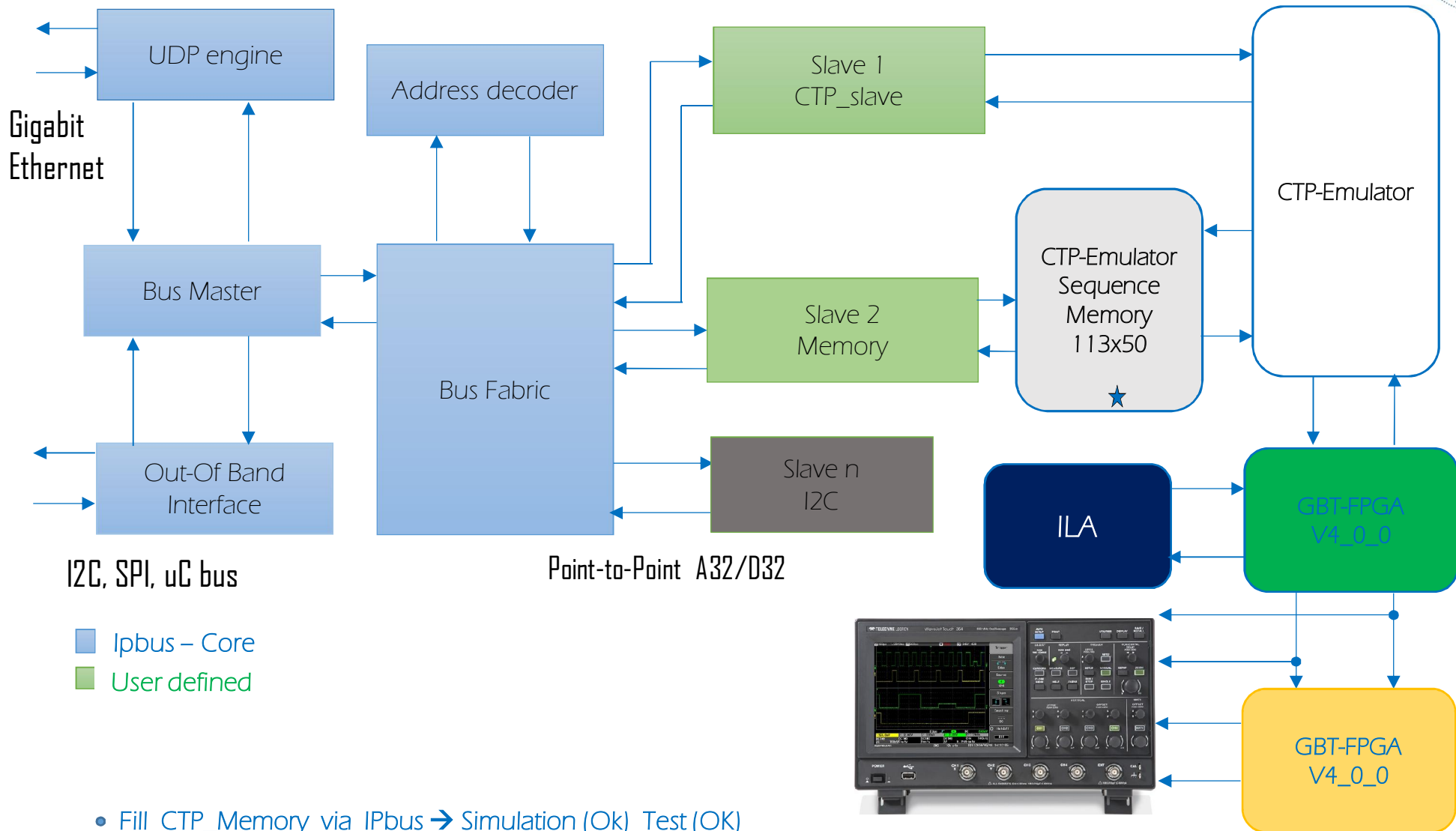
-  A.Fernández Tellez, M. Rodriguez Cahuantzi, et al, , Analysis id High Muon Multiplicity Cosmic Events with the ALICE Experiment, to be published in Brazilian journal of Physics. (Proceeding os the Astroparticle Physics Conference 2013, 2-9 July, Rio de Janeiro, Brazil).
-  B. Abelev, A. Fernández Téllez, M. Rodriguez Cahuantzi, Guillermo Tejeda Muñoz, M. Martínez Hernández, ALICE Collaboration , Centrality dependence of Pion, Kaon, and Proton Production in Pb-Pb Collisions at  $\sqrt{s_{NN}} = 2.76$  TeV, Phys. Rev. C 88, 044910 (2014).
-  B. Abelev, A. Fernández Téllez, M. Rodriguez Cahuantzi, Guillermo Tejeda Muñoz, M. Martínez Hernández, ALICE Collaboration , Multiplicity dependence of two-particle azimuthal correlations in pp collisions at the LHC, JHEP09(2015)049.
-  A. Fernández Téllez, M. Martínez Hernández, M. Rodriguez Cahuantzi, The ALICE Collaboration, Technical Design Report on Forward Detectors: FMD, T0 and V0. CERN\*-LHCC-2004-025
-  M.Krivda, A. Jusko, O.Villalobos Baillie: The ALICE trigger electronics. 2010.
-  W.Carena, F.Costa, F.Carena:The ALICE experiment control system. 10th ICALEPCS, 2011.



▶ Back Up

E-mail: [lperezmo@cern.ch](mailto:lperezmo@cern.ch).





I2C, SPI, uC bus

Point-to-Point A32/D32

- Ipbus – Core
- User defined

- Fill CTP\_Memory via IPbus → Simulation (Ok) Test (OK)
- GBT\_V4\_0\_0 → Simulation (Ok) Test (OK)

