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Hybrid Photo Detector as the Ashra trigger sensor

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Abstract: We have developed a Hybrid Photo Detector (HPD) for the Ashra detector. The HPD consists of a 6-inch electron tube and a multi-pixel silicon detector followed by trigger decision LSI circuits. The advanced features of the silicon detector are as follows: 1. high resolution with 64×64 channels using bump bonding technique 2. high gain due to a thin dead layer and a large effective area 3. fast response due to electron collection. We report the designs and performance of the HPD in this contribution.

Introduction

Ashra (All-sky Survey High Resolution Air shower detector) [1],[2],[3] is a new detector to detect UV, Cherenkov and fluorescence light. To detect rare cosmic ray events from large background events, a sophisticated trigger is indispensable. We have applied the techniques matured in the fields of image intensifier, solid state image sensor and CMOS LSI circuit [4],[5],[6],[7] to the Ashra trigger sensor.

Fig 1. shows overview of the photoelectric image pipeline of the Ashra detector. Size of incoming image is reduced with an Image Intensifier (I.I.) and amplified with another I.I. Then the light is split into three ways; one for a commercial CCD chip on a board to catch untriggered light images continuously, another for two trigger sensors and the other for a CMOS image sensor which has 2048×2048 pixels. The trigger sensor employs a Hybrid Photo Detector (HPD) with 64×64 pixels and finds a rough position of light to be measured. The incident light to the trigger sensor is split into two HPDs in order to process Cherenkov light and fluorescence light independently. Light to the CMOS image sensor is delayed by another I.I. to make delay for trigger decision time using the scintillation light on phosphor P46, of which 10%-decay-time is 200 ns. The CMOS image sensor opens a shutter for corresponding region with a 1st trigger signal made by the trigger sensor. After more elaborated trigger processing, 2nd trigger signal is issued for a real event candidate. With the 2nd trigger signal, the image sensor outputs data to the data acquisition system.

Requirements for the HPD as the Ashra trigger sensor are as follows: 1. the anode is pixelized with an enough resolution to recognize an image pattern of cosmic ray event. 2. signal and background can be discriminated with high efficiency within the trigger decision time (200 ns). 3. signal of the events with different time scale such as Cherenkov light (a few tens of ns) and fluorescence light ($\sim$ 10 μs) can be processed. The design and performance of the HPD are discussed in this contribution.

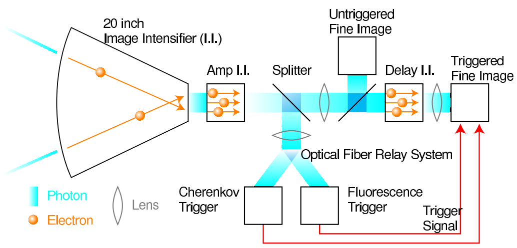

Figure 1: Photoelectric image pipeline of the Ashra detector.

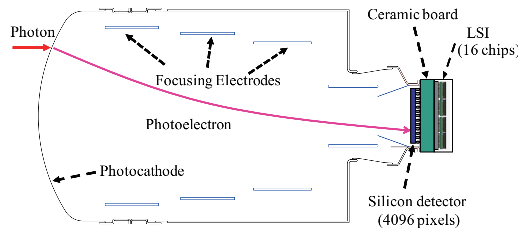

Figure 2: Schematic of the pixel HPD.

Figure 3: Photograph of a prototype HPD.

Hybrid Photo Detector

The HPD consists of an electron tube and a multi-pixel silicon detector followed by trigger decision LSI circuits as shown in Fig 2.

Fig 3. shows a photograph of a prototype HPD. The electron tube uses an entrance window of a 3 mm thick glass with a photocathode. The effective diameter at the entrance window is 152.4 mm. Photoelectrons are accelerated by the "cross-focusing" electric field formed by high voltages applied to the photocathode and electrodes. When applying voltage of -25 kV to the photocathode, a photoelectron produces a signal of about 6000 electrons in the silicon detector. The demagnification factor is five and the spatial granularity is about 2.2 mm $\times$ 2.2 mm at the entrance window of the electron tube.

The silicon detector has 64 $\times$ 64 pixels, and its pixel size is 450 μm $\times$ 450 μm. The size of the silicon detector is 30.8 mm $\times$ 30.8 mm and the thickness the substrate is 250 μm.

We used an high resistivity ($\sim$ 2 k$\Omega\cdot$ cm) n-type silicon wafer of <111> orientation as a substrate of the silicon detector. The p+ layer was made on the front surface and 64 $\times$ 64 electrodes were made on the rear surface by ion implantation. By applying a reverse bias voltage of about 85V, the silicon detector is used as a fully depleted sensor. Current of each electrode of the silicon detector is injected to LSI circuits through bump bonds and electrical feedthroughs which are hermetically sealed on a ceramic board. By the device simulation of the silicon detector, low crosstalk, a rising time of 4 ns and dark current of the order of 1 nA, which is much lower than expected signal current (more than 1 μA /pixel), are obtained.

Trigger LSI circuits

The trigger LSI chip is used to receive electric currents from the silicon detector and to send trigger signal of position of light to be measured by the CMOS sensor. Fig 4. shows a photograph of the LSI chip. The LSI chips were fabricated in a commercial 0.35 μm CMOS process and each LSI chip has 16 $\times$ 16 pixels. The chip size is 9.8 mm $\times$ 9.8 mm and the pixel size is 500 μm $\times$ 500 μm.

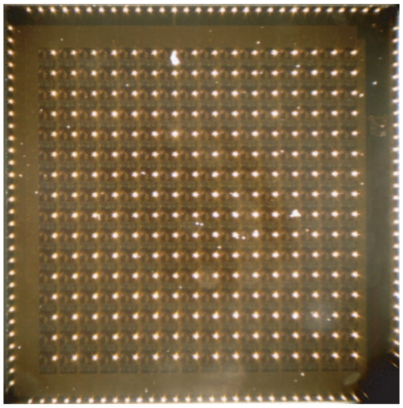

Figure 4: Photograph of the LSI chip.

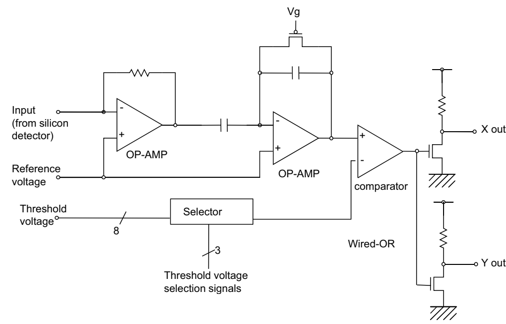

Figure 5: Schematic of the pixel architecture in the LSI chip.

Totally 4096 channels on 16 LSI chips are implemented on the backside of the ceramic board.

The chip must discriminate between signal and background noise with high efficiency and send binary signal to the CMOS image sensor within a trigger decision time. The schematic of the pixel architecture in the LSI chip is shown in Fig 5. The output current of the silicon detector is converted to a voltage, filtered by the bandpass filter and discriminated at a comparator. In order to process different time scale events of Cherenkov light and fluorescence light, bandpass frequency of the filter can be adjusted by an external input voltage. The threshold level on each pixel can be selected from 8 levels to compensate discrepancy, fluctuation of background level and to mask strong light coming from stars or something. The output of discriminators are summed 64 pixels along X and Y axis by using "Wired OR" circuit. The response to rectangular wave on each pixel is measured to be ~ 50 ns. This satisfies the requirement for trigger decision time which is made by using the scintillation light on phosphor P46 at the delay I.I.

Summary

The pixel Hybrid Photo Detector based on technologies matured in the fields of image intensifier, solid state sensor and CMOS LSI is used as the trigger sensor of the Ashra detector. The performance of high resolution and high speed property makes it possible that the CMOS image sensor open a shutter for corresponding region within a trigger decision time. The HPD also reduces the pixel cost comparing to the traditional Cherenkov or fluorescence detector. This will open a new filed "hybrid detection of Cherenkov and fluorescence light with high resolution in wide field-of-view".

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